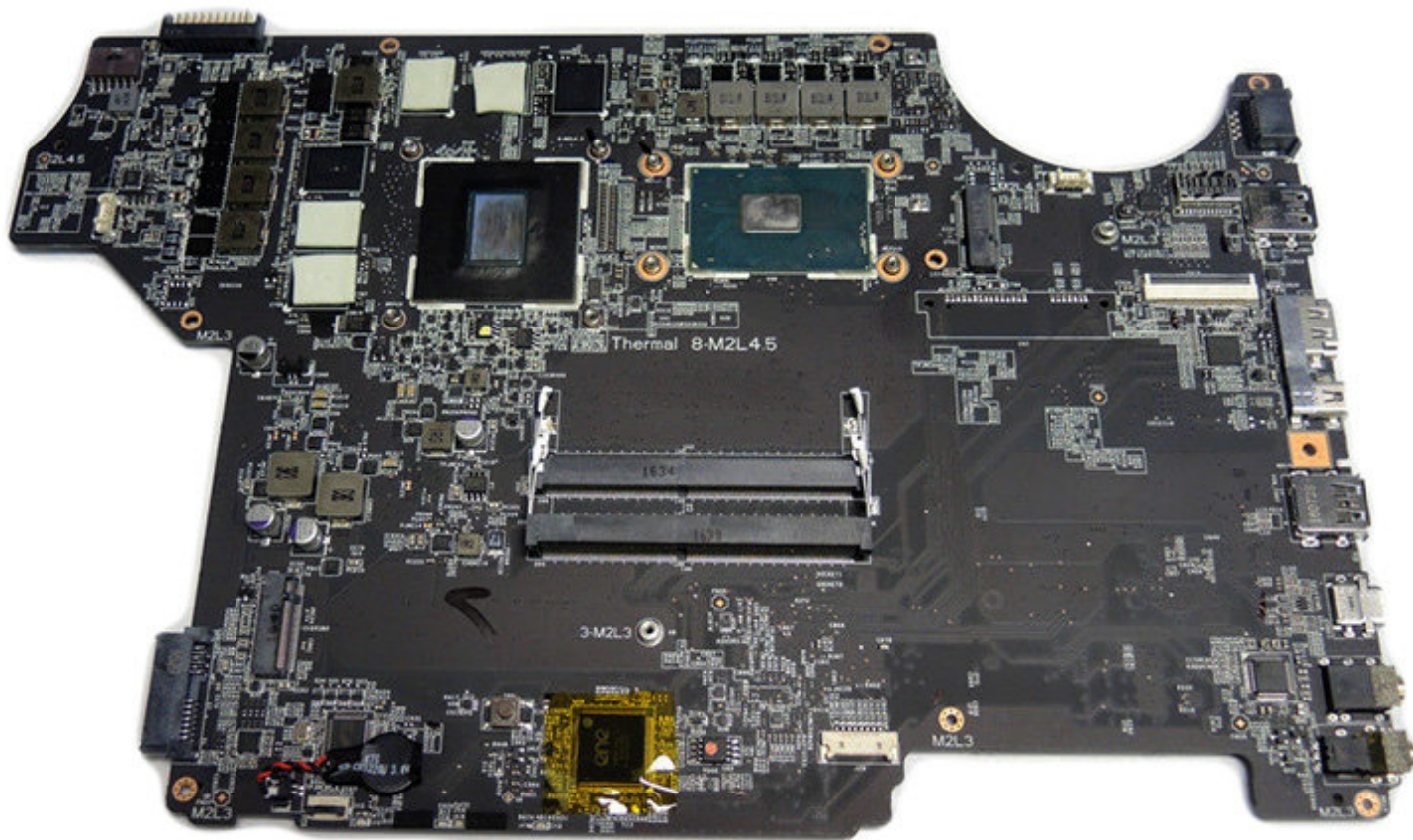




# ***MSI GP62MVR 6RF Leopard Pro***

**MS-16JB1 ver 1.0**

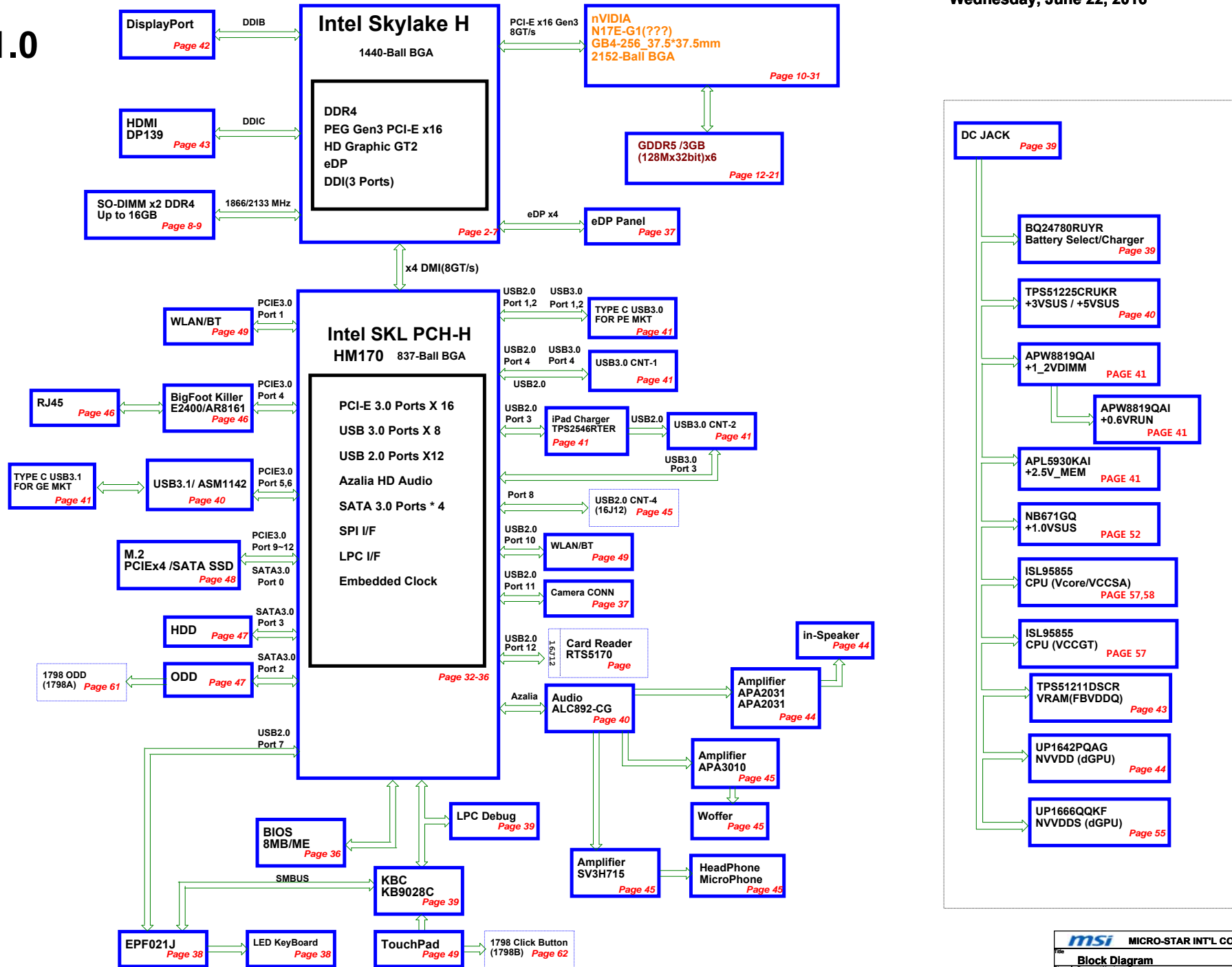


# MS-16JB/MS-179B

## Intel Skylake Mobile

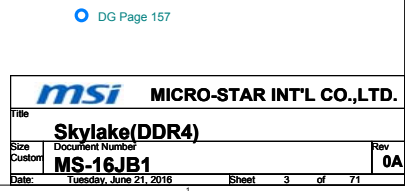
Ver:1.0

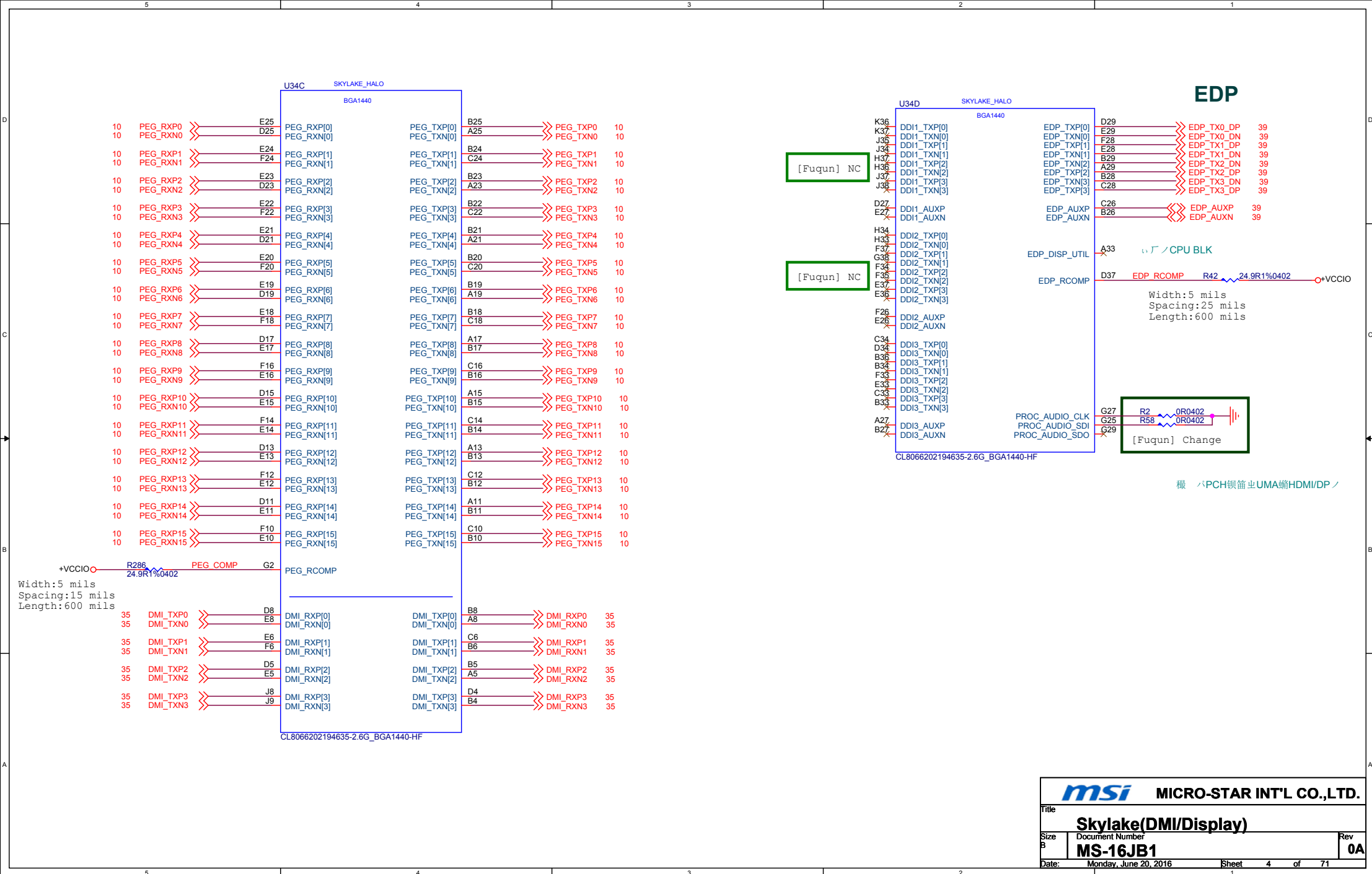
Wednesday, June 22, 2016



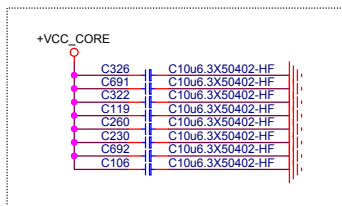
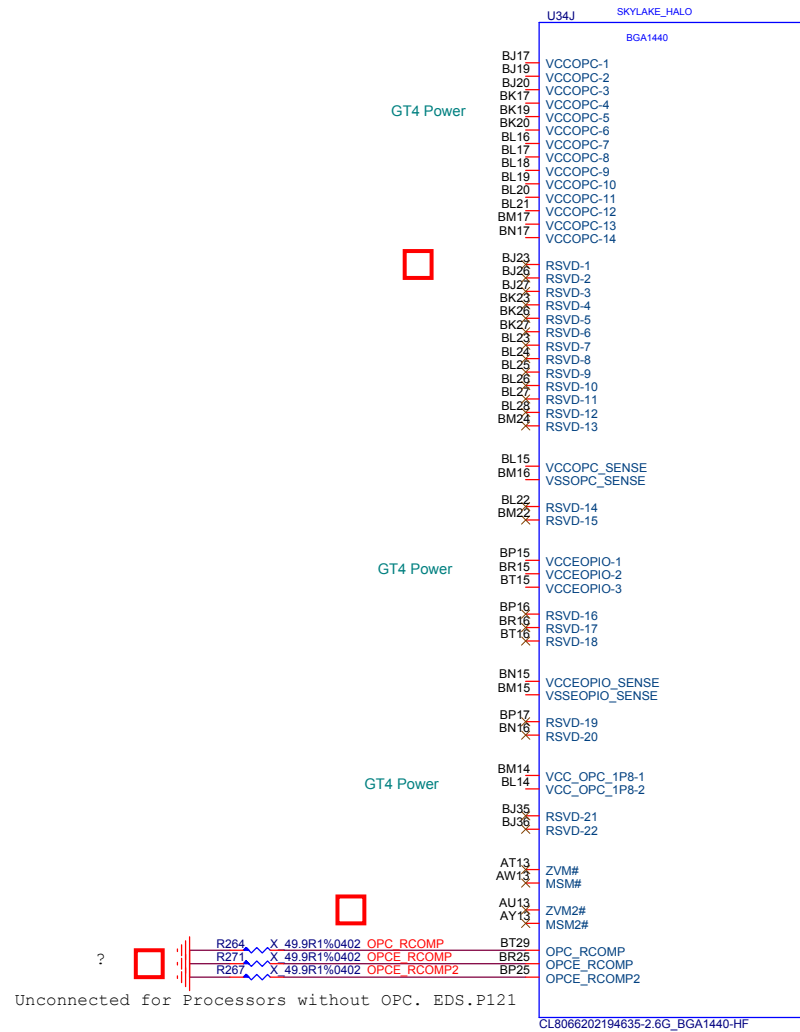
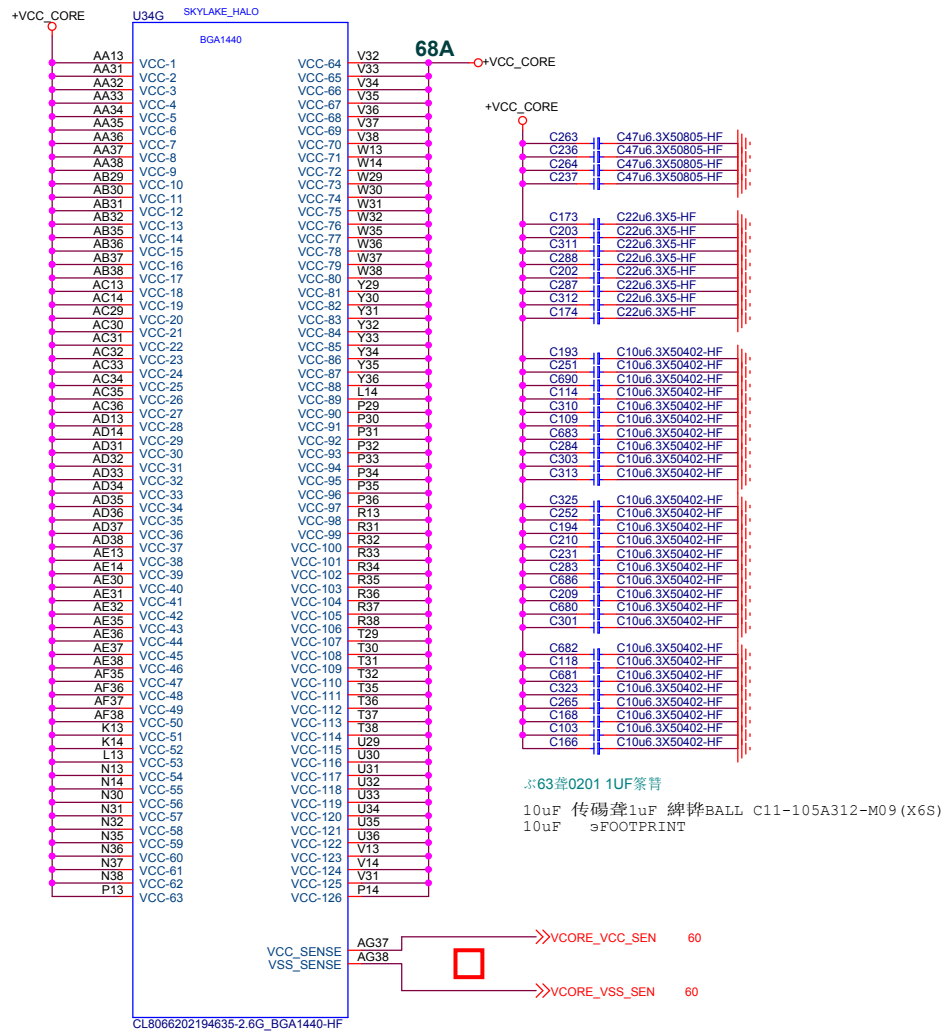


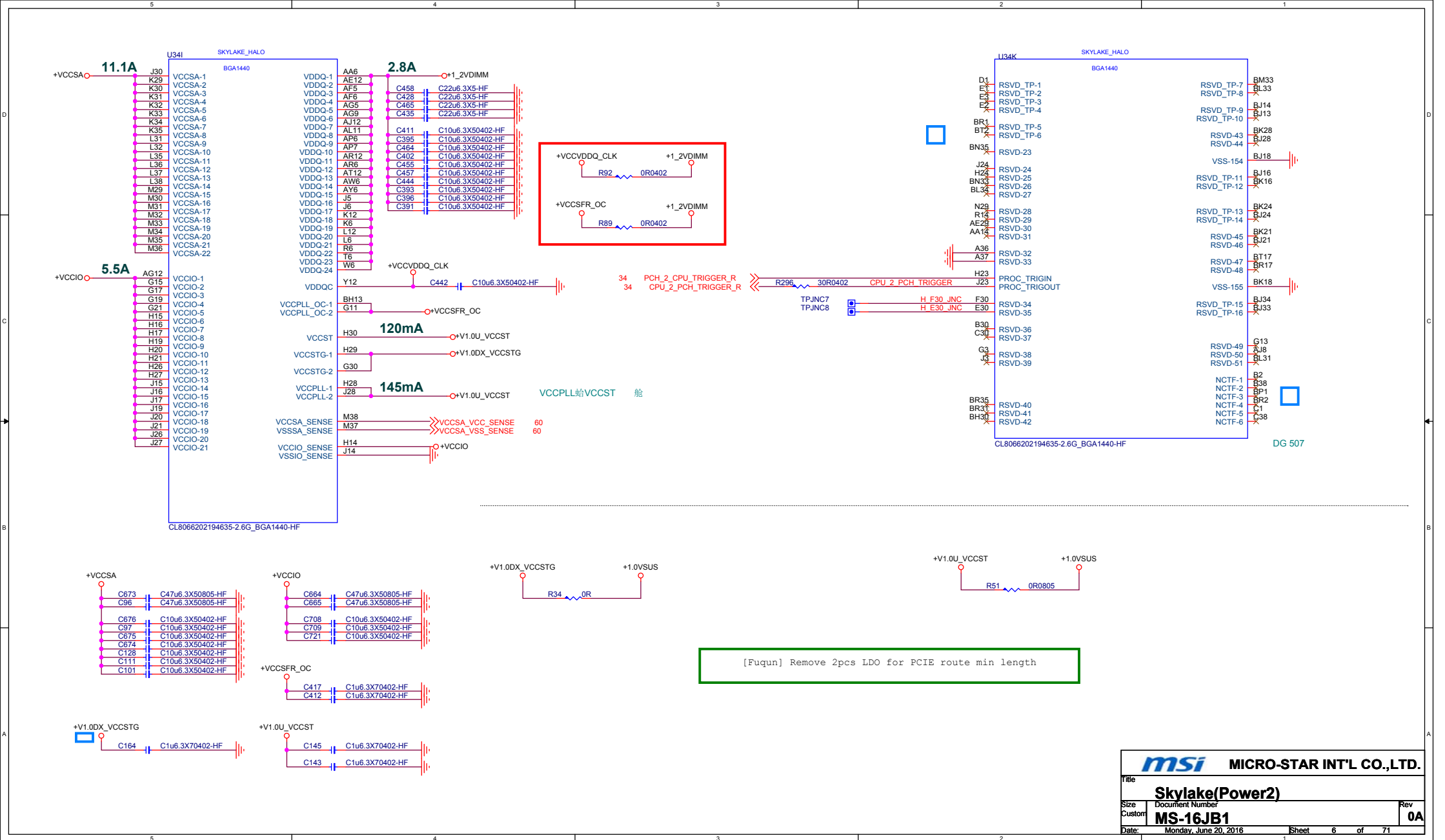
## DDR Channel B









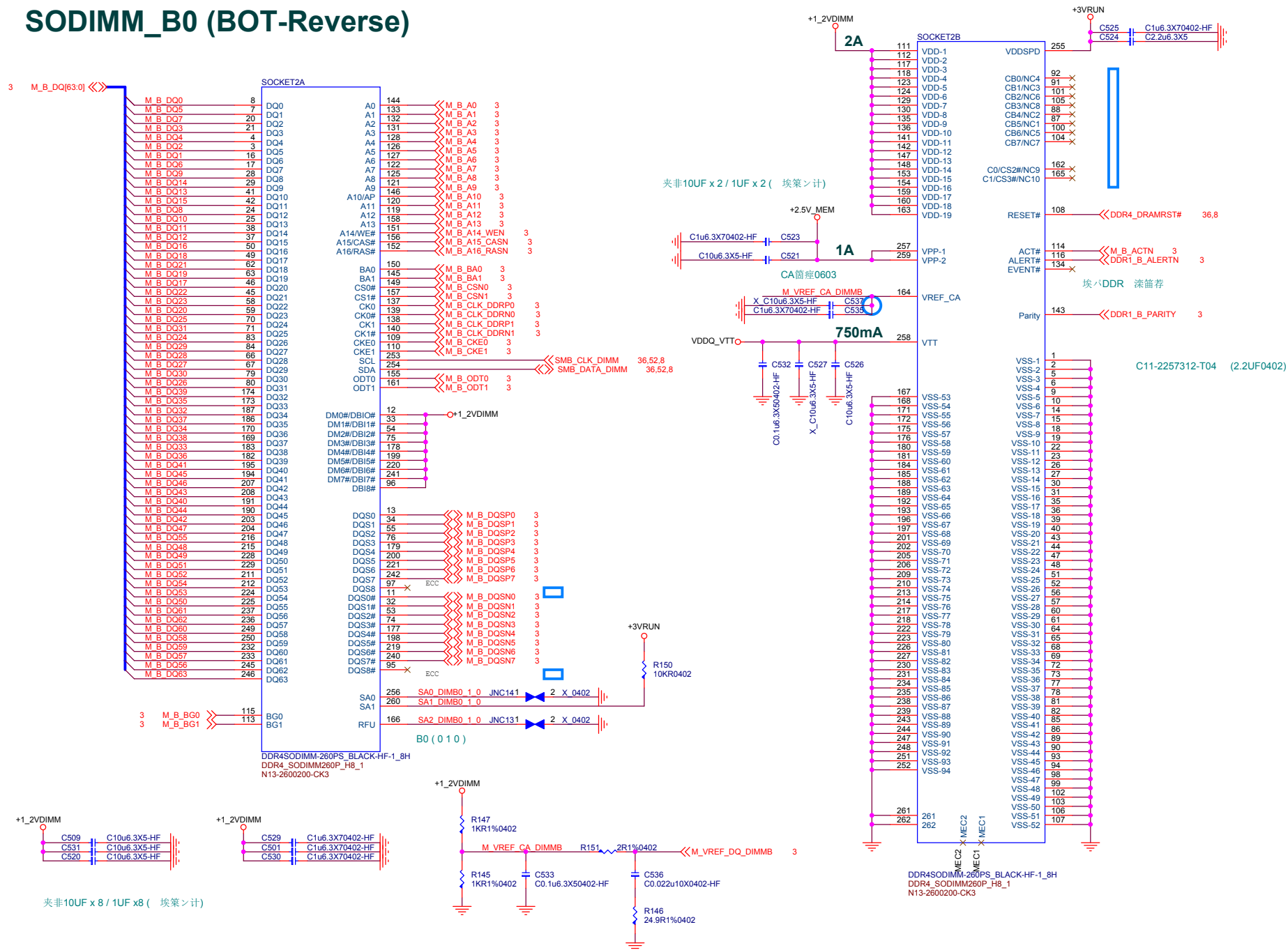








# SODIMM\_B0 (BOT-Reverse)



# GPU PCI EXPRESS

## Close Balls

## Outside of BGA

1uF\*4 X6S

4.7uF\*2 X6S

10uF\*4 X6S 4V

22uF\*4 X5R

C11-106A233-T04

0.9A

0.1uF\*1 X5R

4.7uF\*2 X6S

Close Balls

Outside of BGA

GPU CLK REQ#

DGPU\_PWRGD

R90

0R0402

PEX\_CLKREQ#

G

Q9

X-N-2N7002\_SOT23

GND

1V8\_MAIN

[Fuqun] Change 1V8\_AON to 1V8\_MAIN for GC6

[Fuqun] Add

PEX\_CLKREQ#

Q47

N-AO3414\_SOT23-3-RH

msi

MICRO-STAR INT'L CO.,LTD.

Model DGPU PCI-E Host

Size MS-16JB1

Date: Monday, June 20, 2016

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Rev 0A

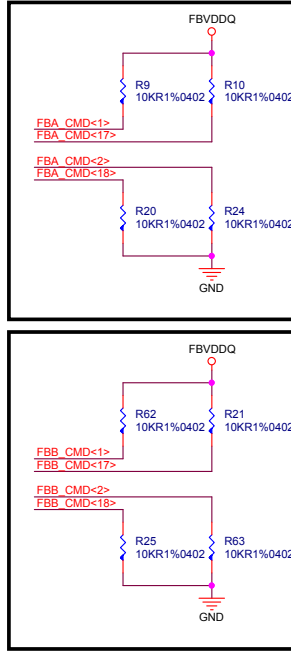
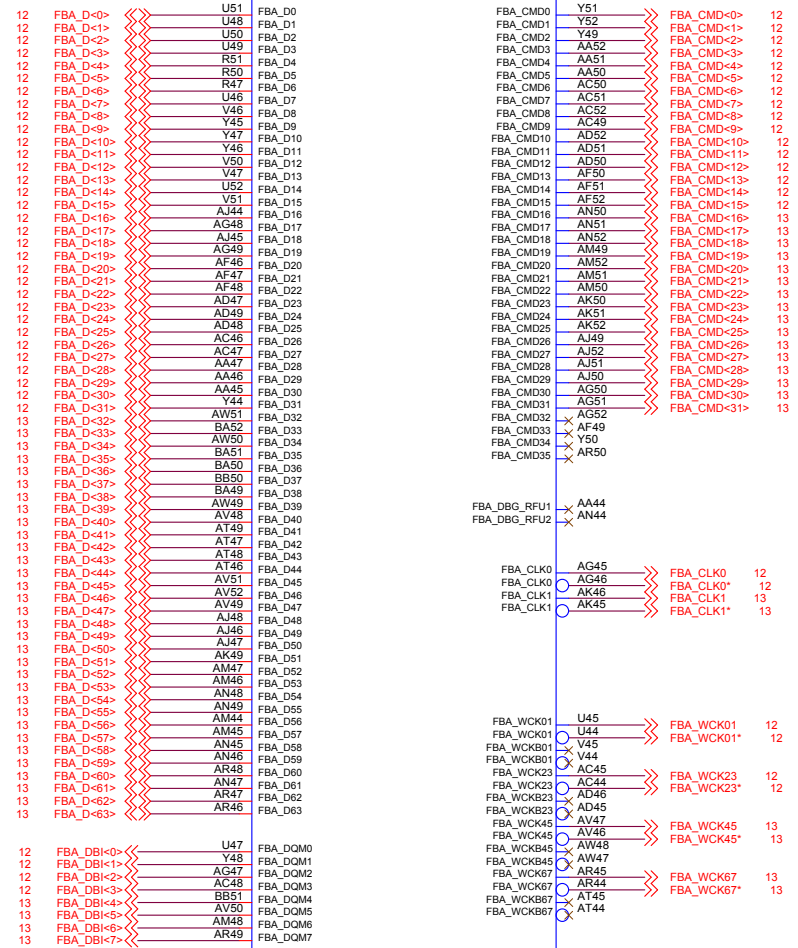
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G7B  
INS205021791

2/23 FBA

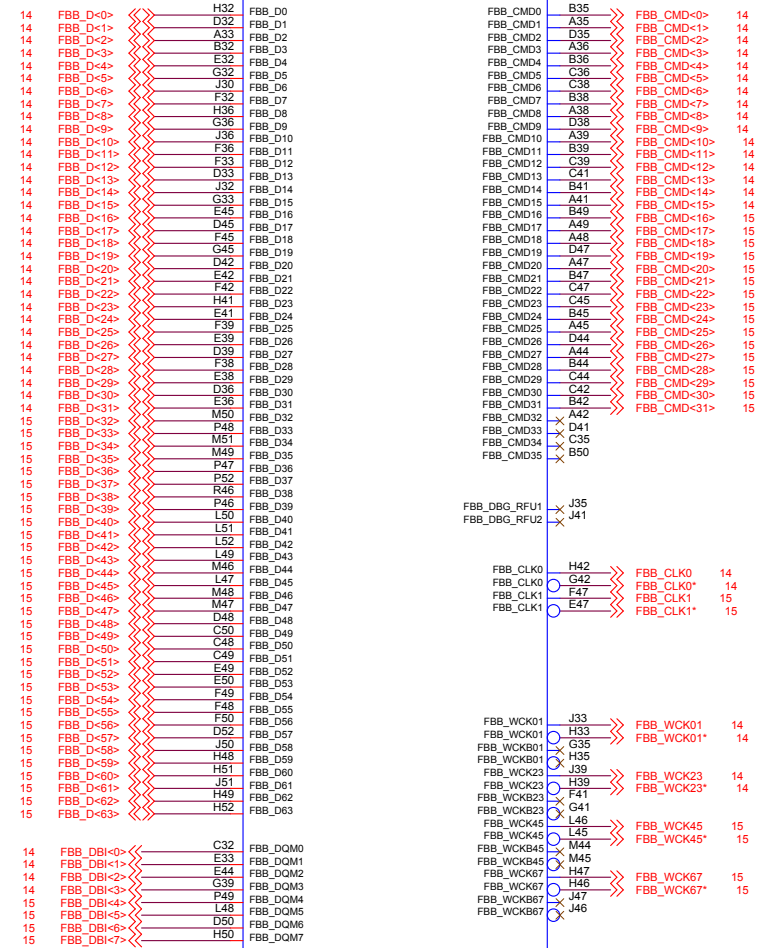
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3/23 FBB

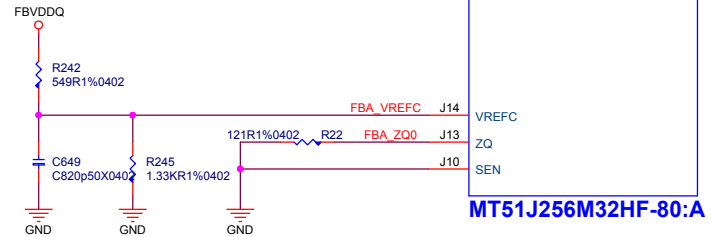
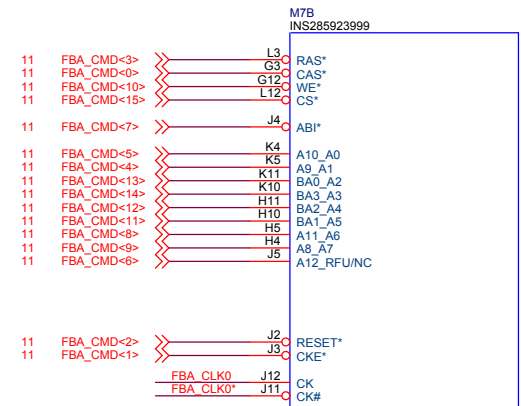
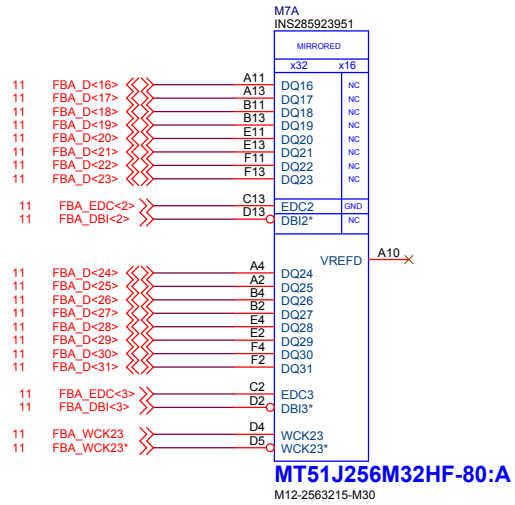


GDDR5 Mode F Mapping By GB3-256

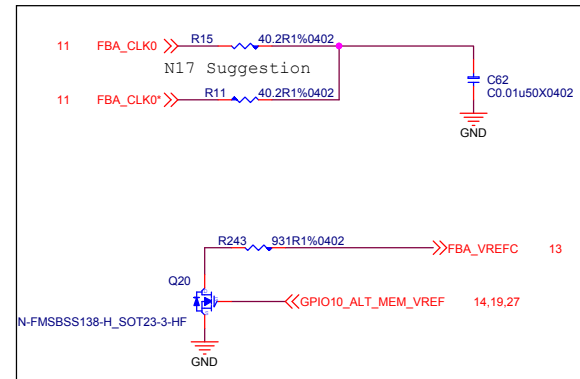
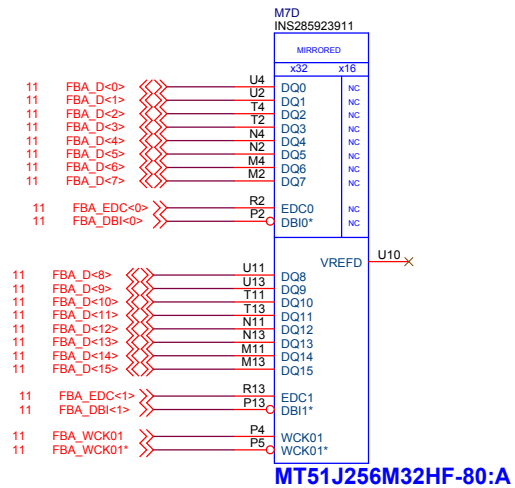
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CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1 A9	
CMD5	A0 A10	
CMD6	A12 RFU	
CMD7	AB1	
CMD8	A6 A11	
CMD9	A7 A8	
CMD10	WE*	
CMD11	A5 BA1	
CMD12	A4 BA2	
CMD13	A2 BA0	
CMD14	A3 BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1 A9
CMD21		A0 A10
CMD22		A12 RFU
CMD23		AB1
CMD24		A6 A11
CMD25		A7 A8
CMD26		WE*
CMD27		A5 BA1
CMD28		A4 BA2
CMD29		A2 BA0
CMD30		A3 BA3
CMD31		CS*



# DGPU\_GDDR5 FrameBuffer A0

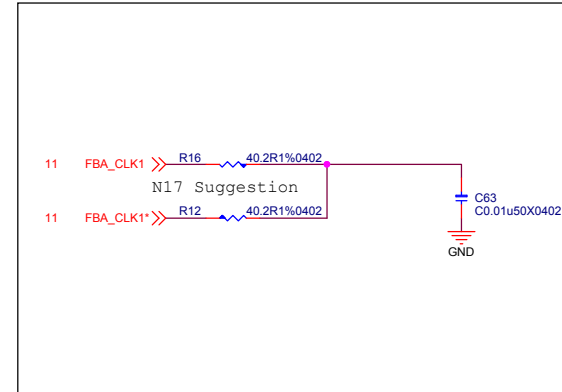
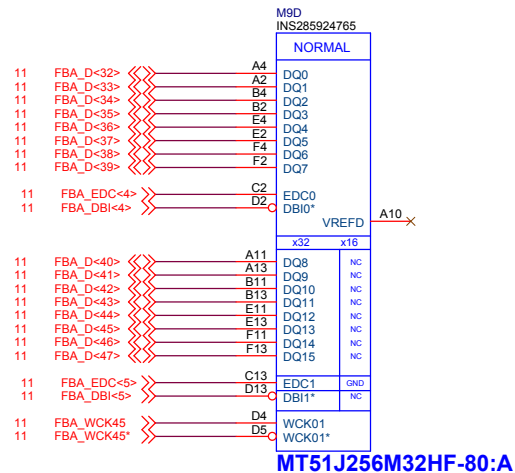
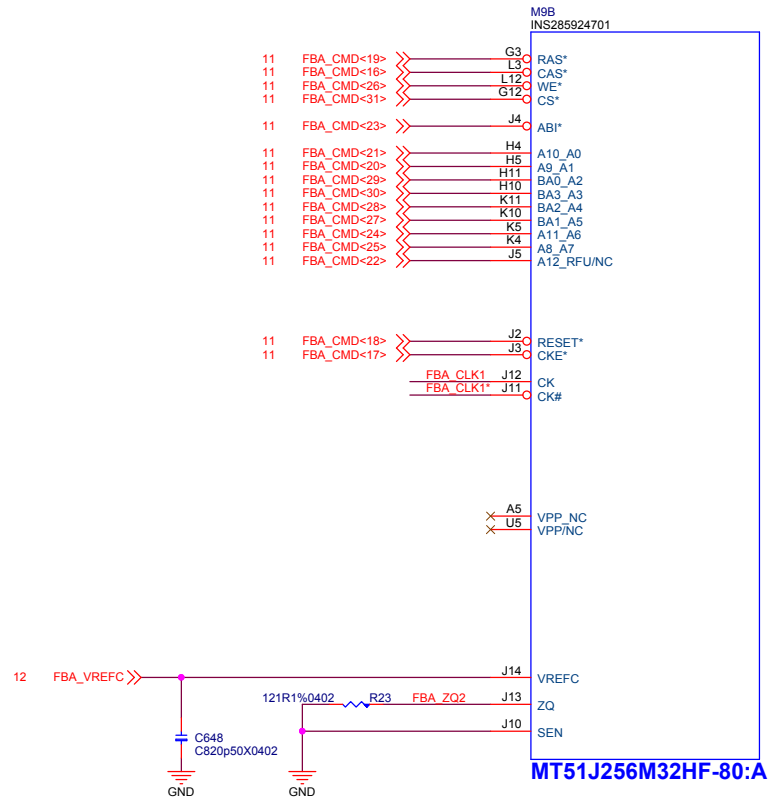
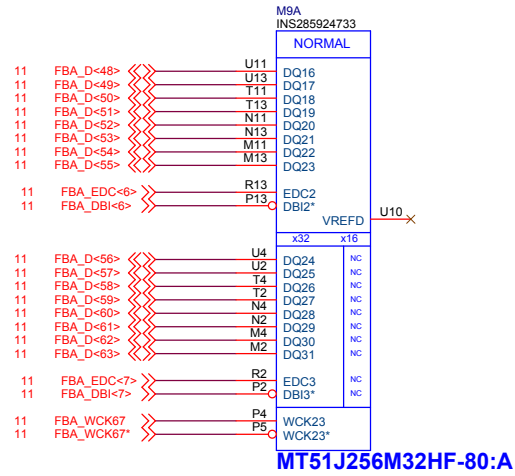


[Fuqun] R245 footprint C0402\_MXM\_1 ?





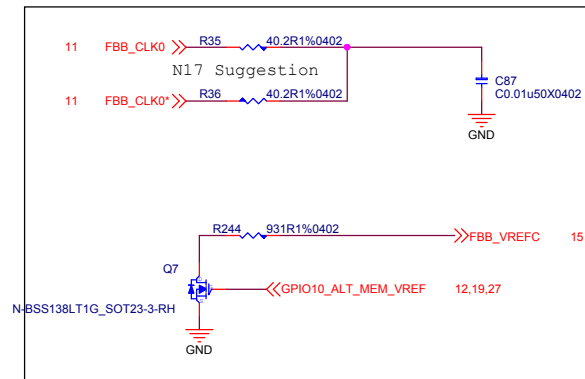
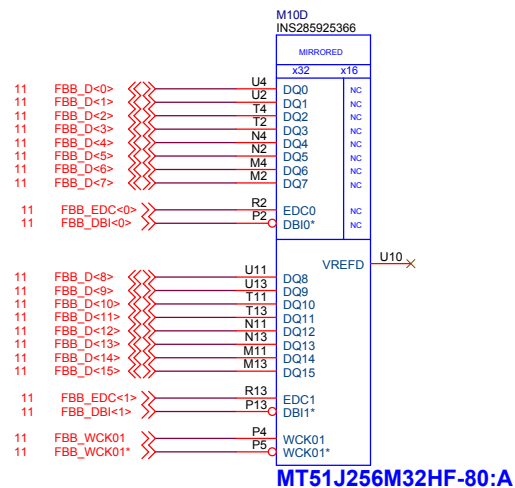
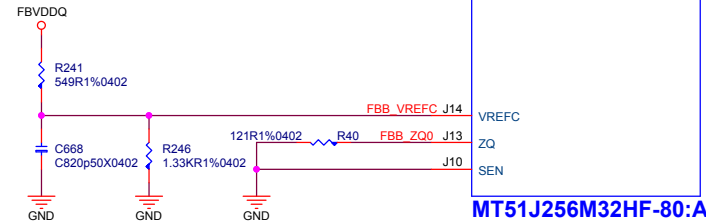
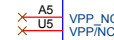
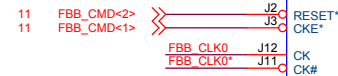
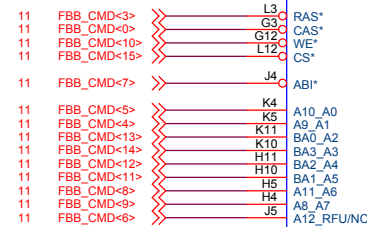
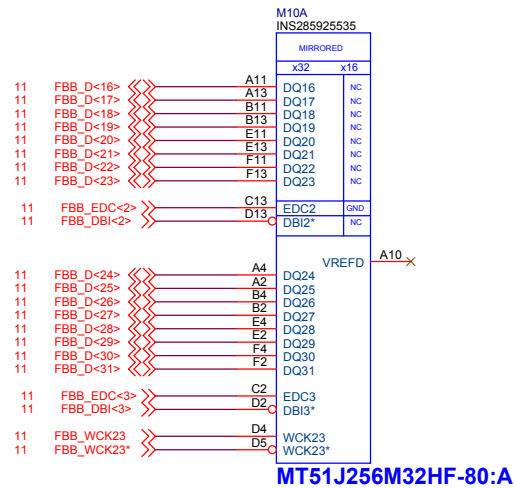
# DGPU\_GDDR5 FrameBuffer A1



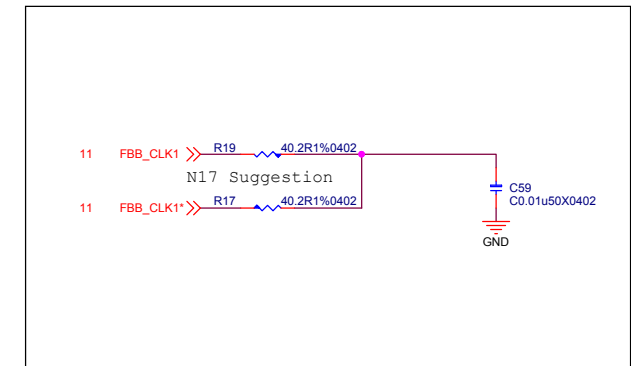
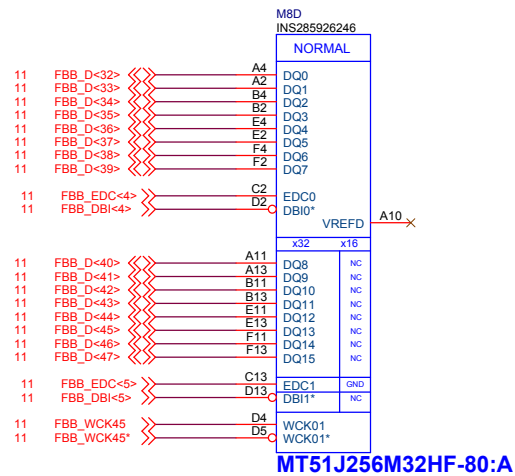
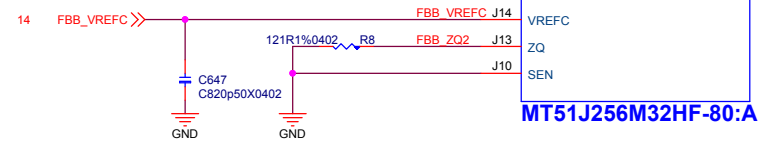
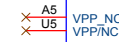
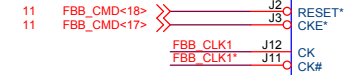
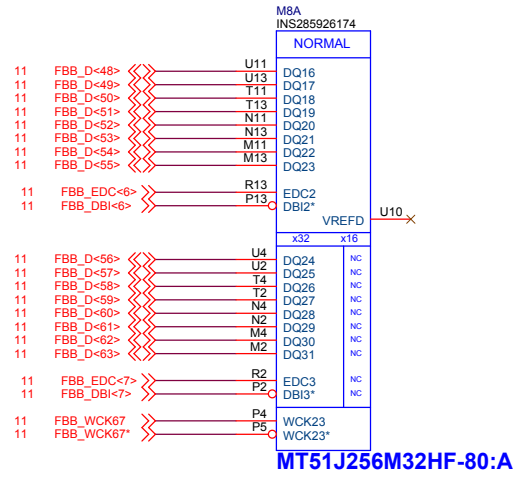
Micron PN :M12-2563215-M30 / MT51J256M32HF-80:A (256Mx32bit)  
Samsung PN : M12-8032535-S02 / K4G80325FB-HC25 (256Mx32bit)

<b>msi</b> MICRO-STAR INT'L CO.,LTD.	
Title <b>DGPU GDDR5 FrameBuffer A1</b>	
Size	Document Number
<b>MS-16JB1</b>	
Date:	Monday, June 20, 2016
Sheet	13 of 71
Rev	<b>0A</b>

# DGPU\_GDDR5 FrameBuffer B0



# DGPU\_GDDR5 FrameBuffer B1



**msi** MICRO-STAR INT'L CO.,LTD.

Title **DGPU GDDR5 FrameBuffer B1**

Size Document Number **MS-16JB1**

Date: Monday, June 20, 2016

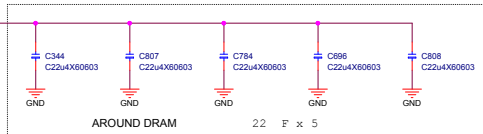
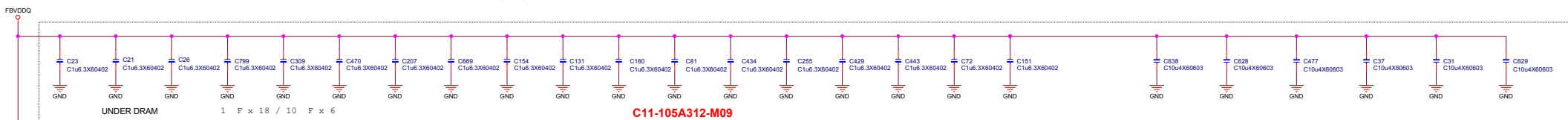
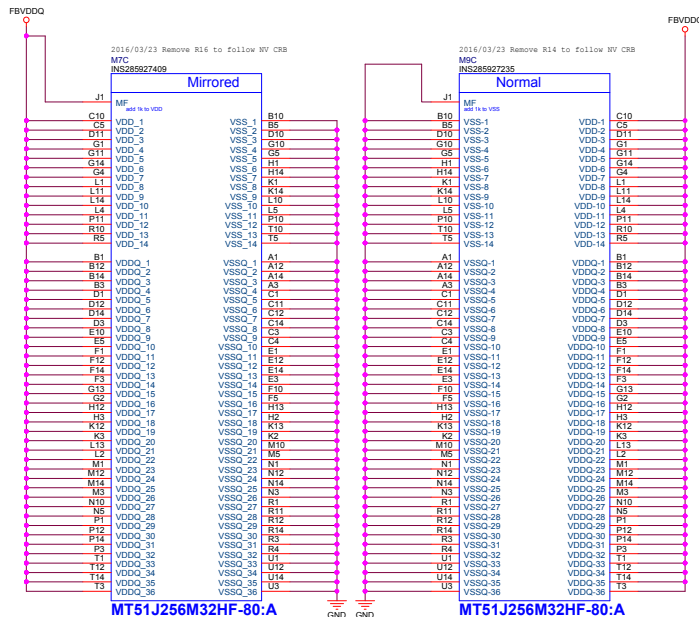
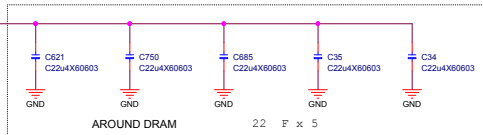
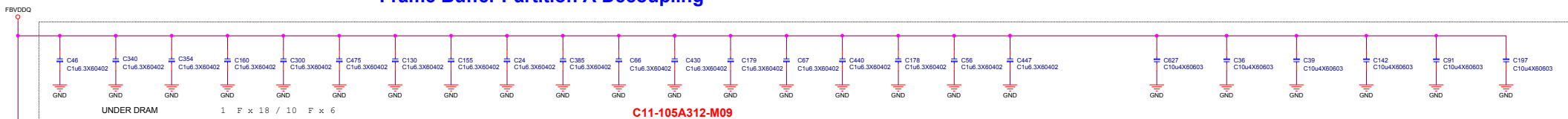
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Rev **0A**

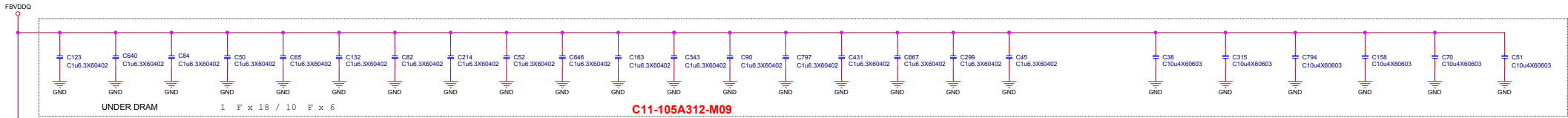
Micron PN :M12-2563215-M30 / MT51J256M32HF-80:A (256Mx32bit)

Samsung PN : M12-8032535-S02 / K4G80325FB-HC25 (256Mx32bit)

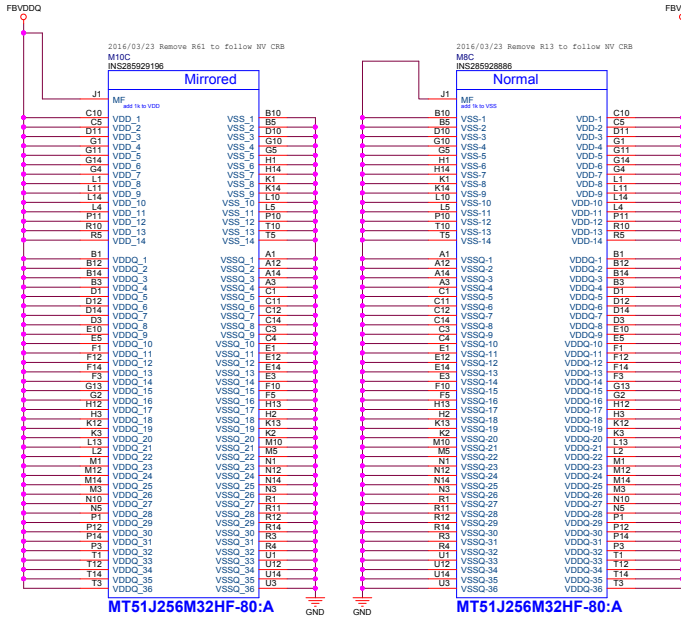
# Frame Buffer Partition A Decoupling



# Frame Buffer Partition B Decoupling

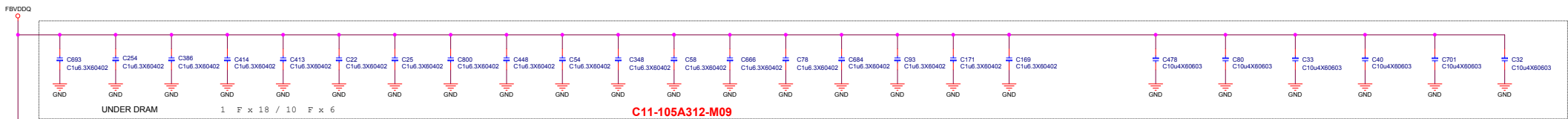


C11-105A312-M09



MT51J256M32HF-80-A

MT51J256M32HF-80-A

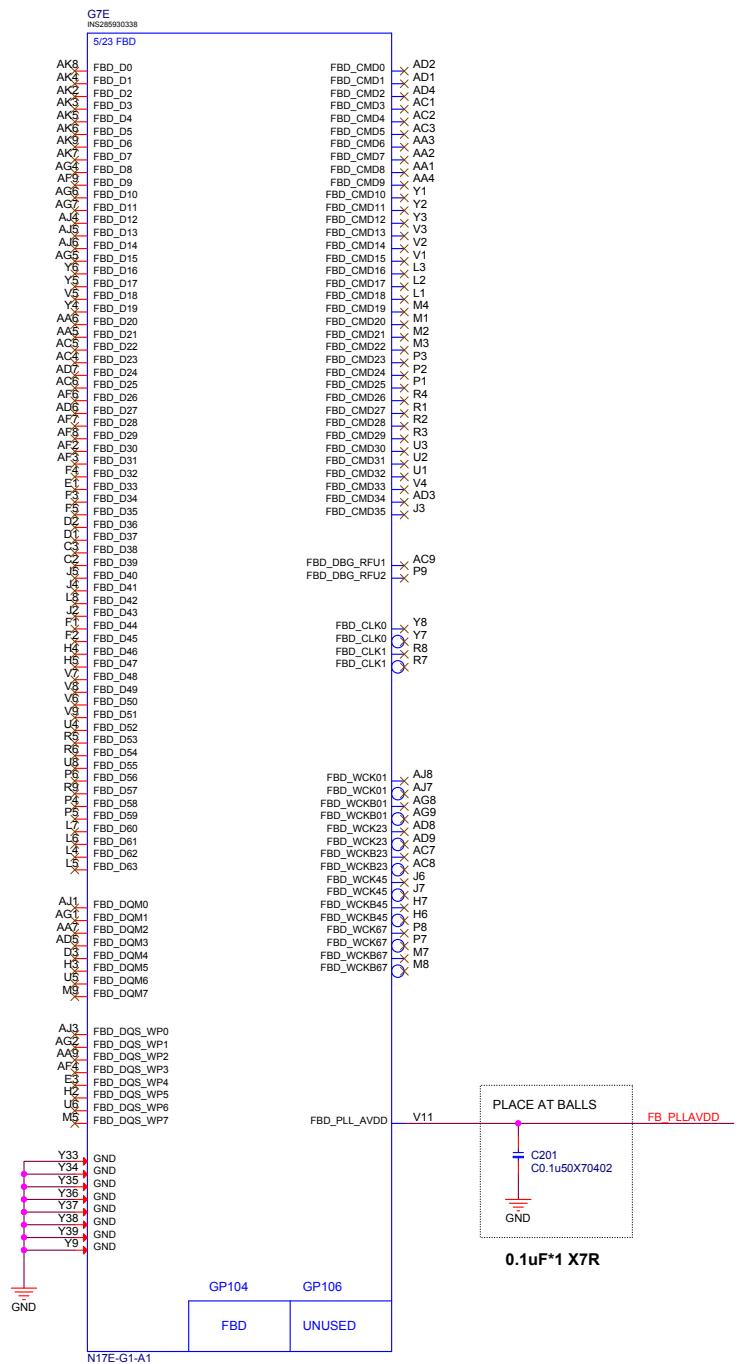


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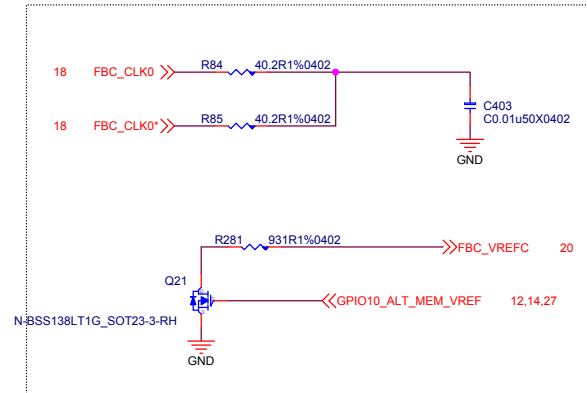
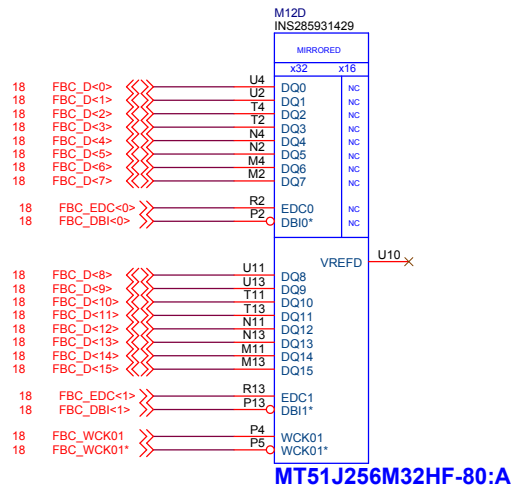
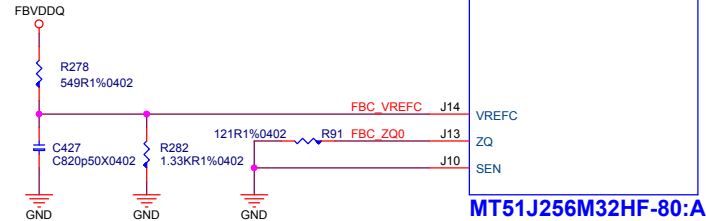
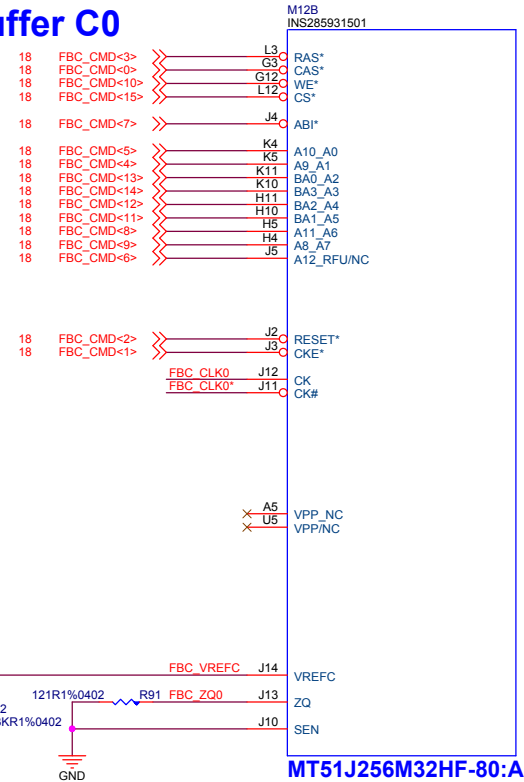
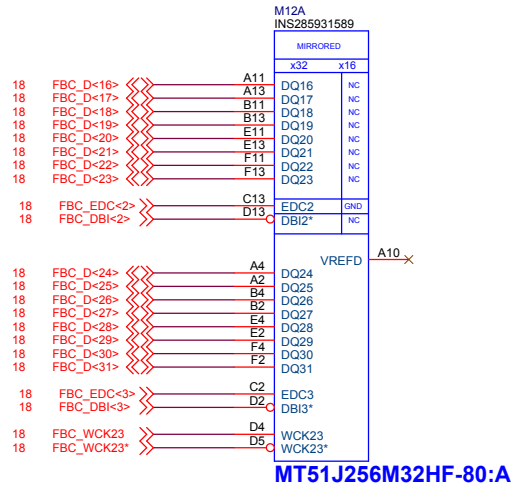




	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A17_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A17_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*



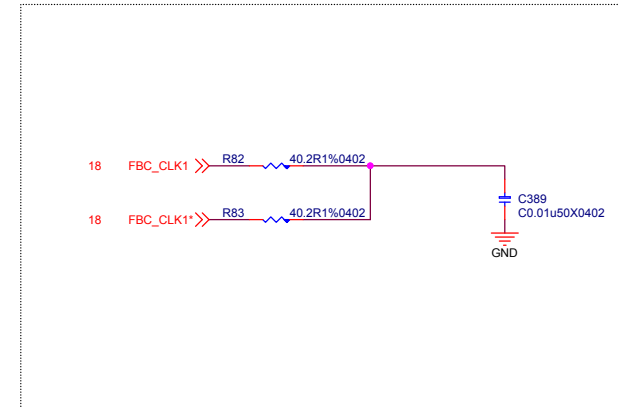
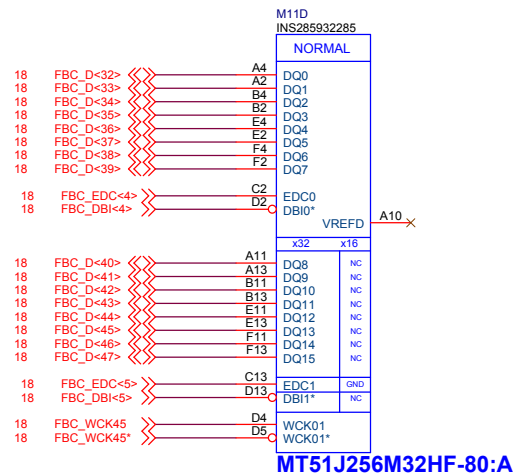
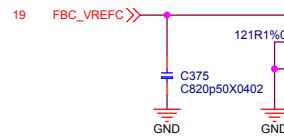
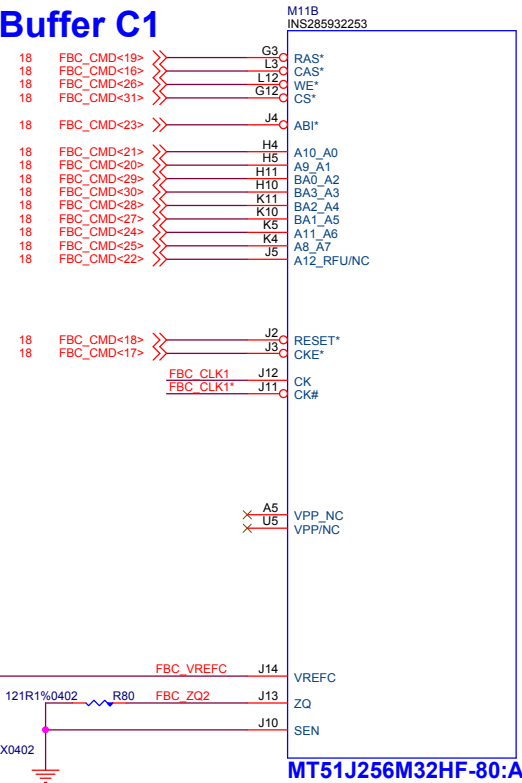
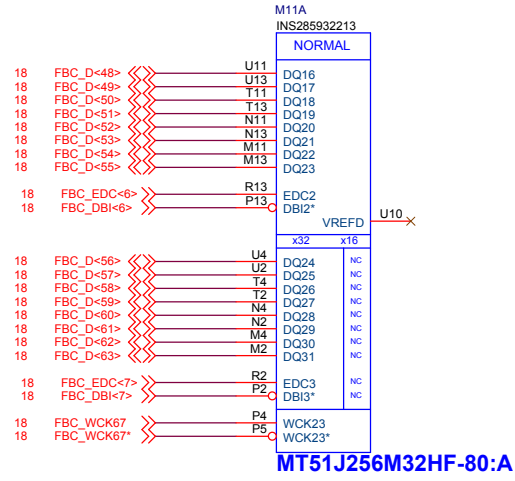
# DGPU\_GDDR5 FrameBuffer C0



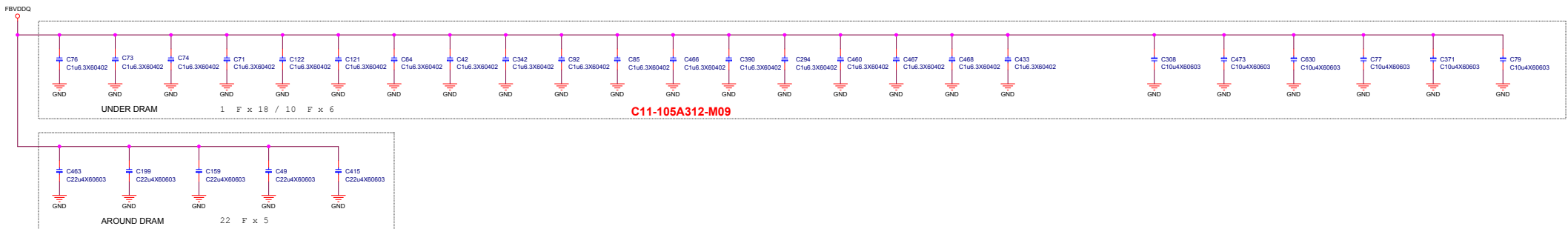
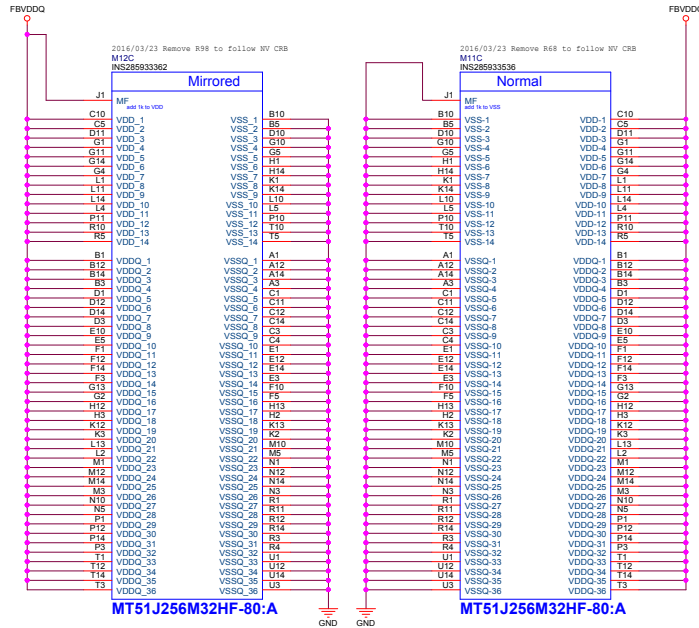
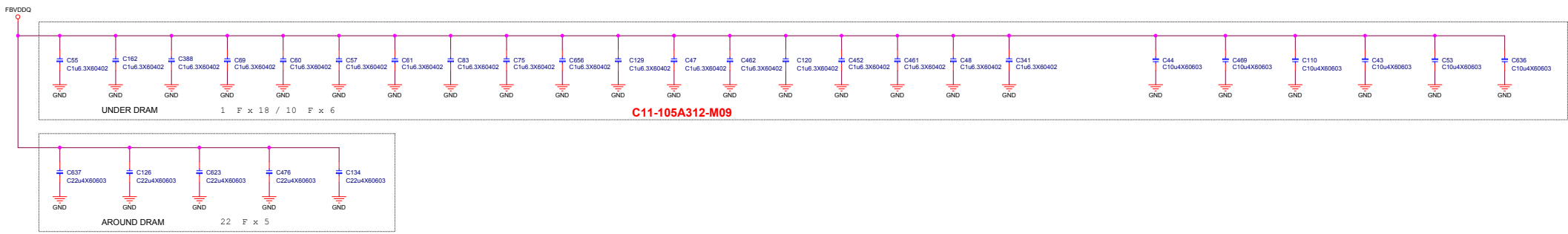
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Title <b>DGPU GDDR5 FrameBuffer C</b>	
Size	Document Number
<b>MS-16JB1</b>	
Date: Monday, June 20, 2016	Sheet 19 of 71
Rev <b>0A</b>	

Micron PN :M12-2563215-M30 / MT51J256M32HF-80:A (256Mx32bit)  
Samsung PN : M12-8032535-S02 / K4G80325FB-HC25 (256Mx32bit)

# DGPU\_GDDR5 FrameBuffer C1



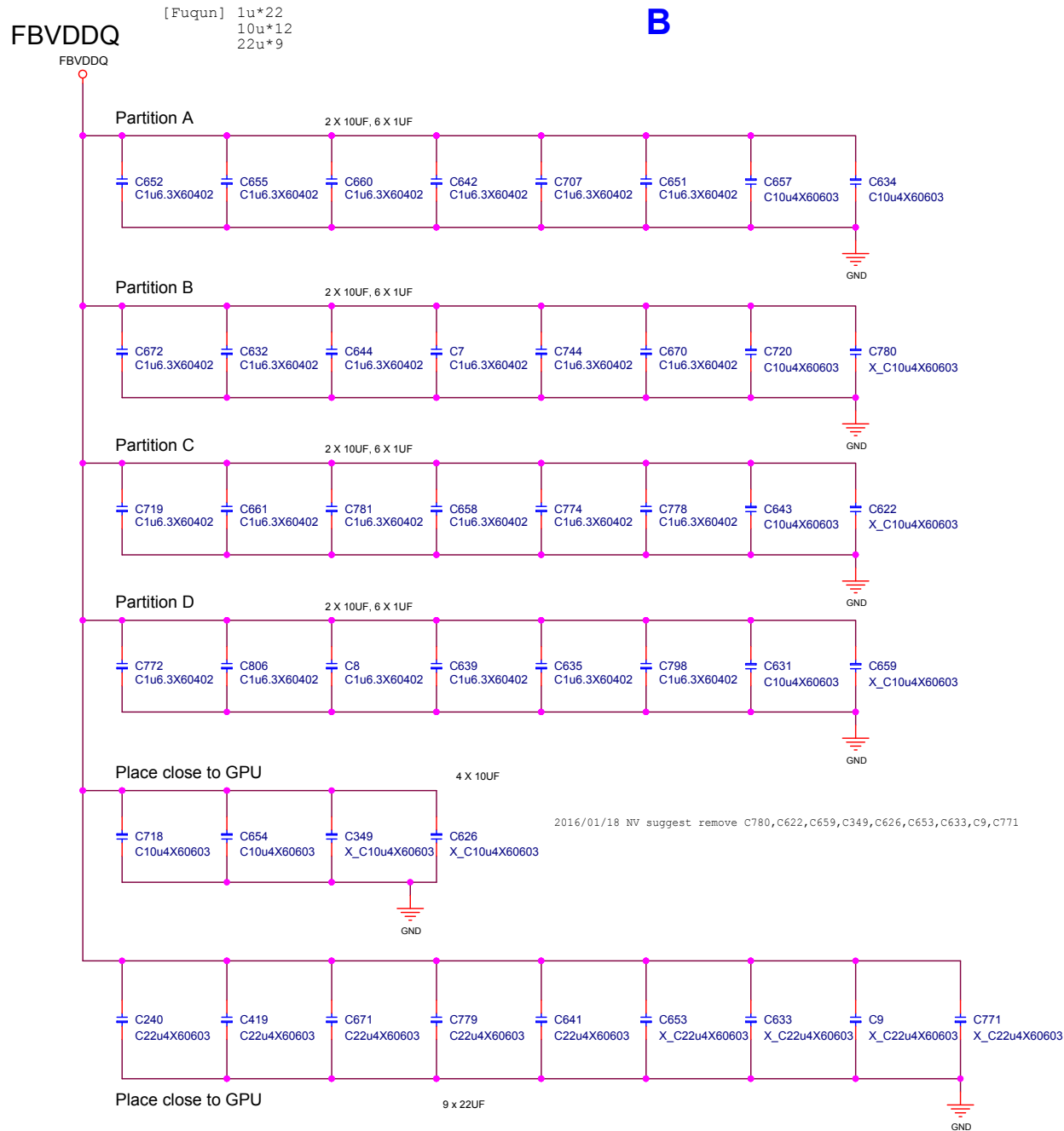
# Frame Buffer Partition C Decoupling



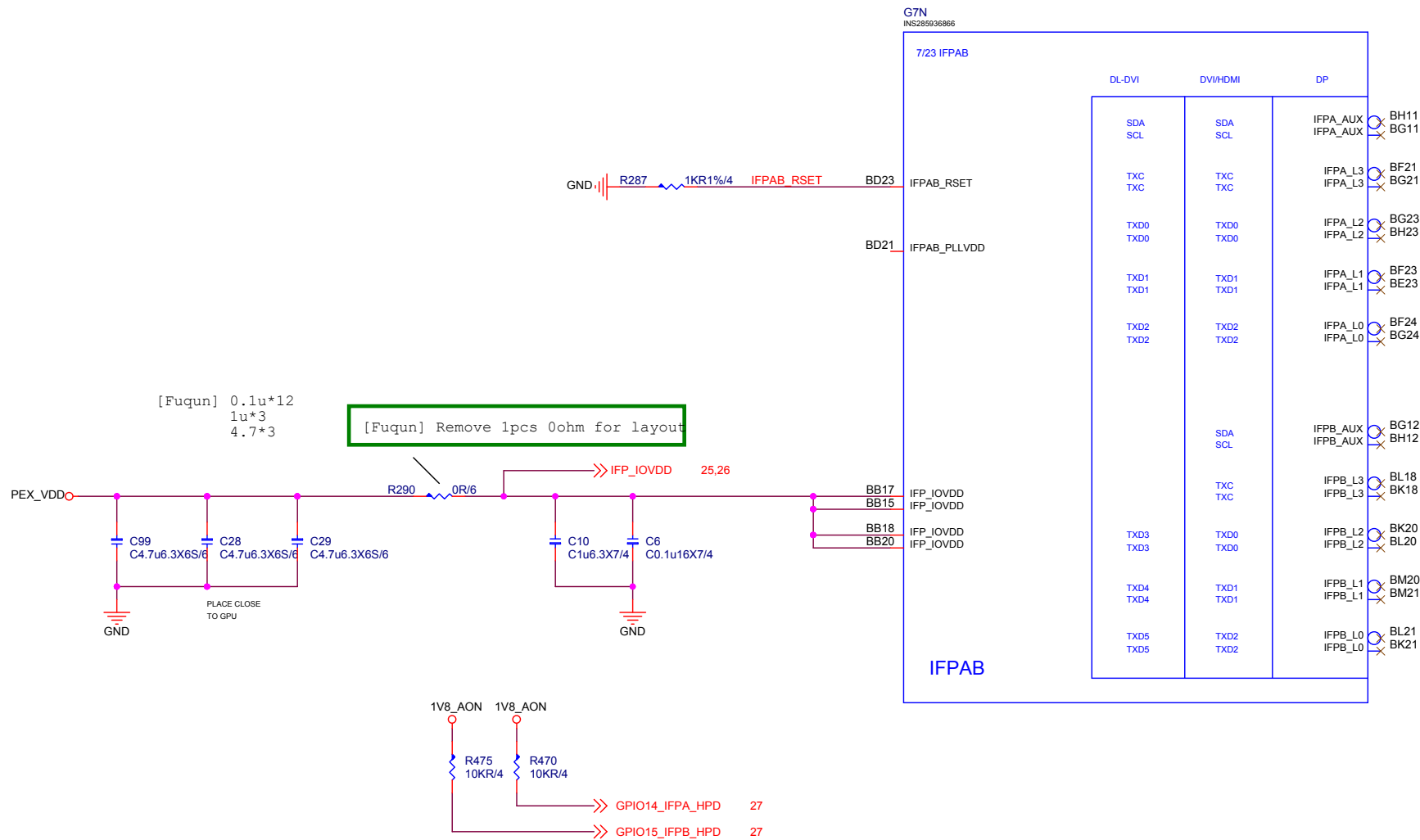




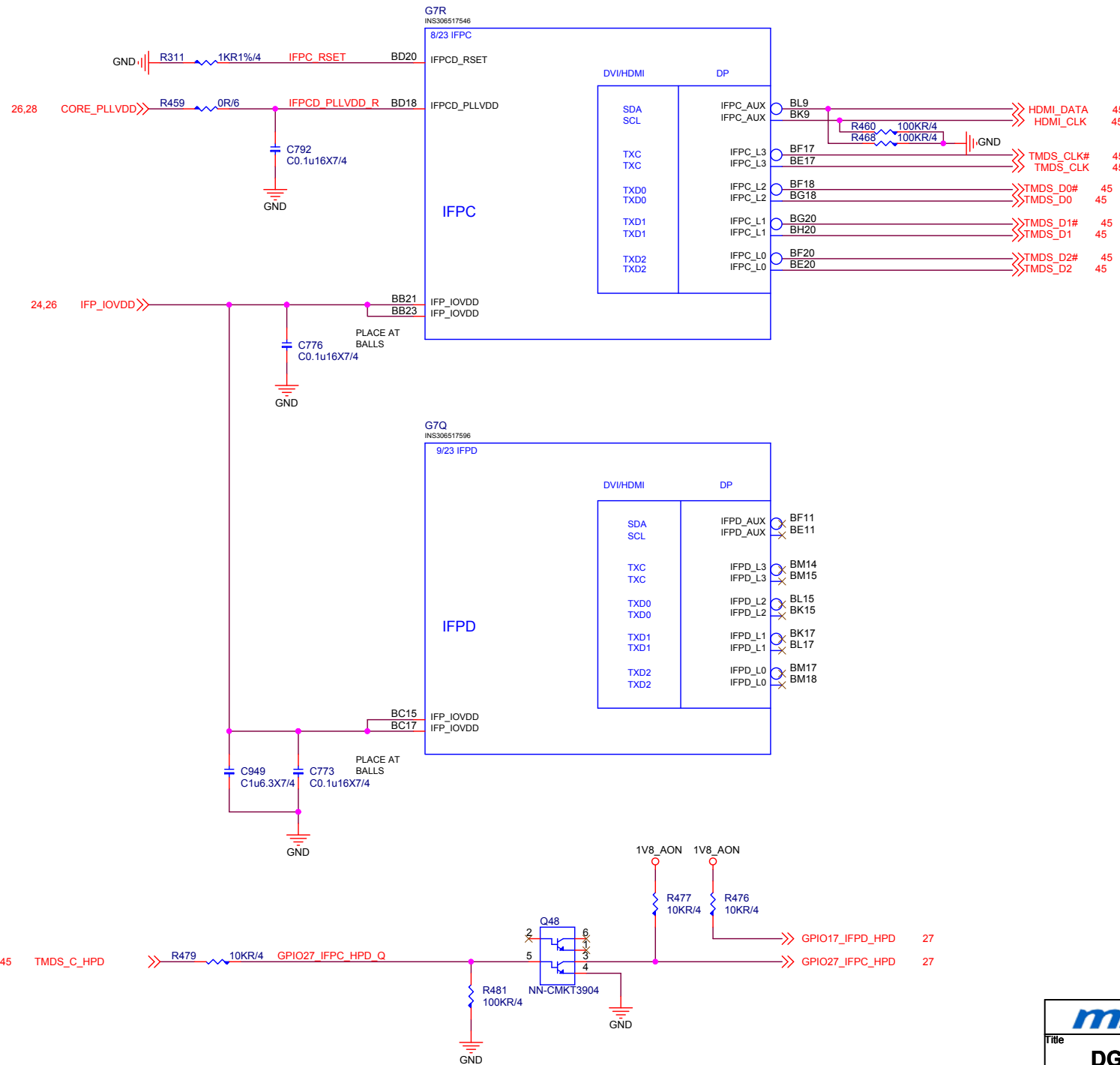
# GPU DECOUPLING B



# IFPCD

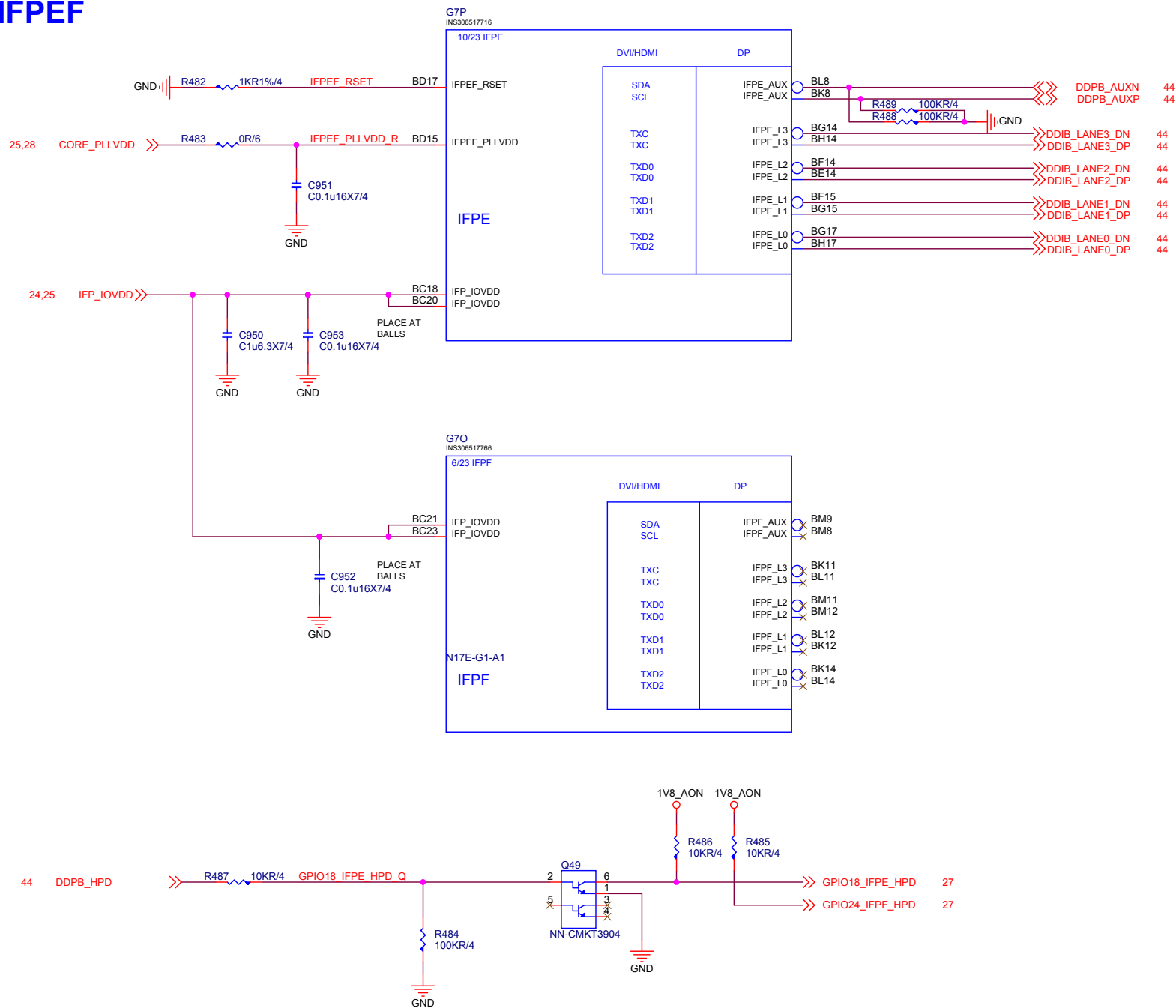


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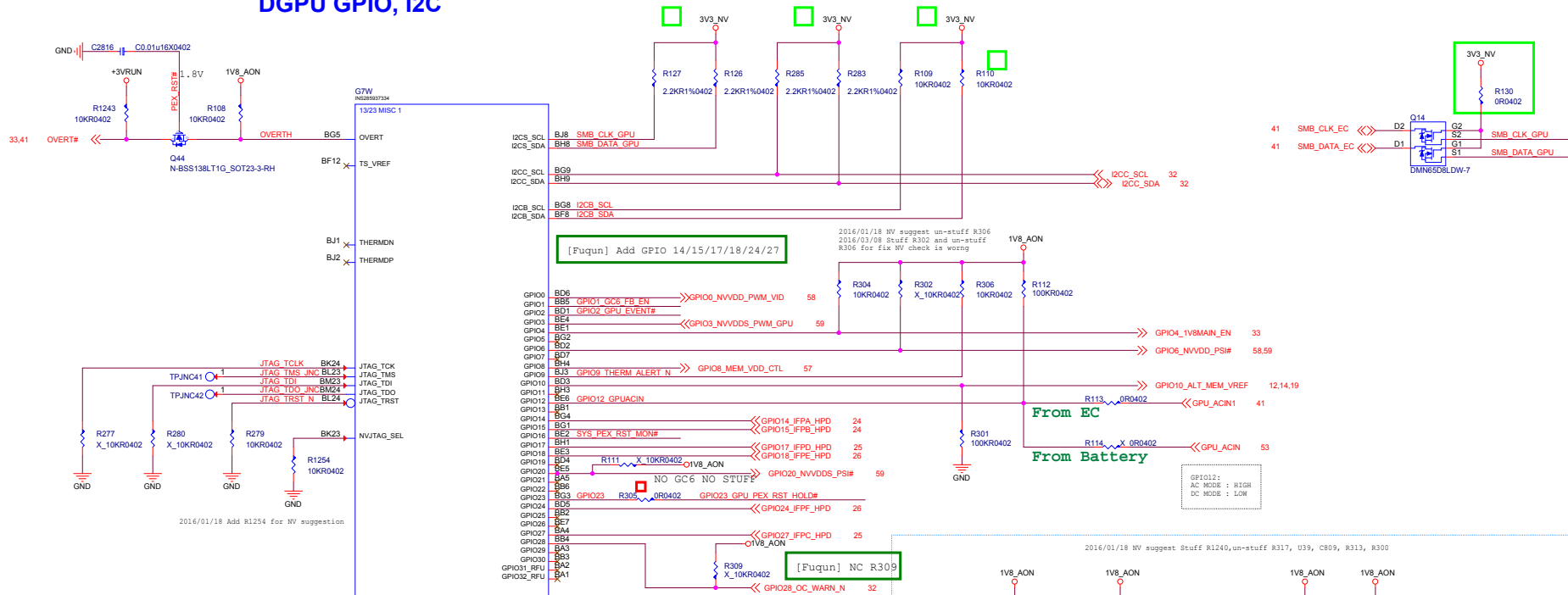


HDMI

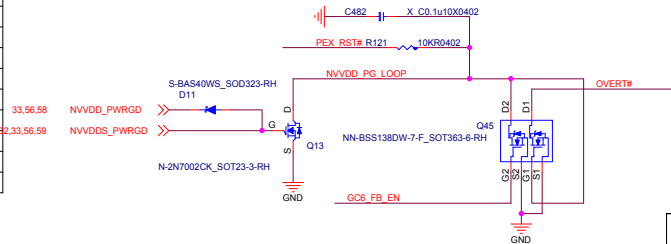
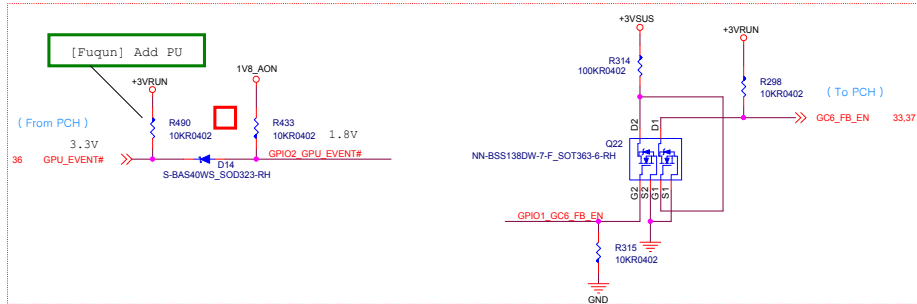
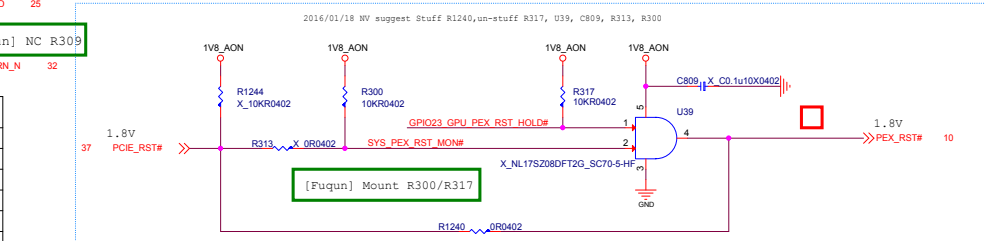
# IFPEF



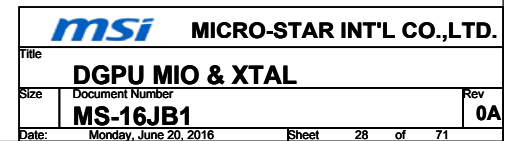
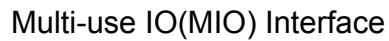
# DGPU GPIO, I2C



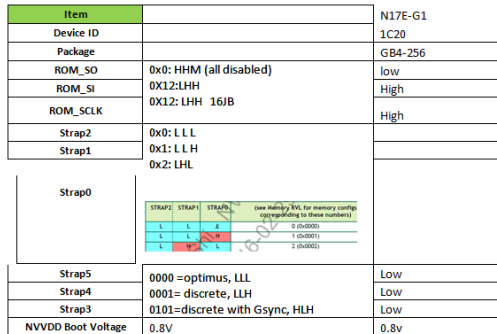
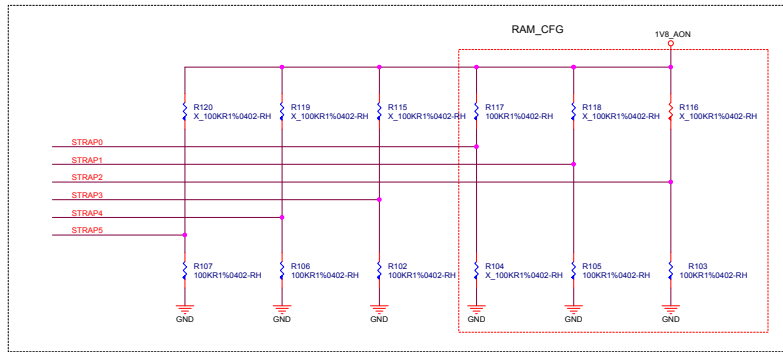
Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8_AON
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	10K pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Fram Lock	1V8 pull-up to 1V8_AON
GPIO6	PSI	O	Phase shedding	10K pull-up to 1V8_AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/O power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 3V3_AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	NVVDD_PSI GC5_MODE	O		
GPIO21	SLI_RASTER_SYNC	I	SLI Raster Sync	100K pull-down
GPIO22	SLI_SWAP_DRY	I	SLI Swap Ready	1K pull-up to 3V3_AON
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIe self-reset control	10K pull-up to 3V3
GPIO24	HPD_F	I	Hot Plug Detect for IFPDF	
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	
GPIO28	OC_WARN	I	Over current throttling	10K pull-up to 1V8_AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	RESERVED			



[Fuqun] Add R492



STRAP0	BL3	STRAP0
STRAP1	BL4	STRAP1
STRAP2	BM4	STRAP2
STRAP3	BM5	STRAP3
STRAP4	BK5	STRAP4
STRAP5	BJ5	STRAP5



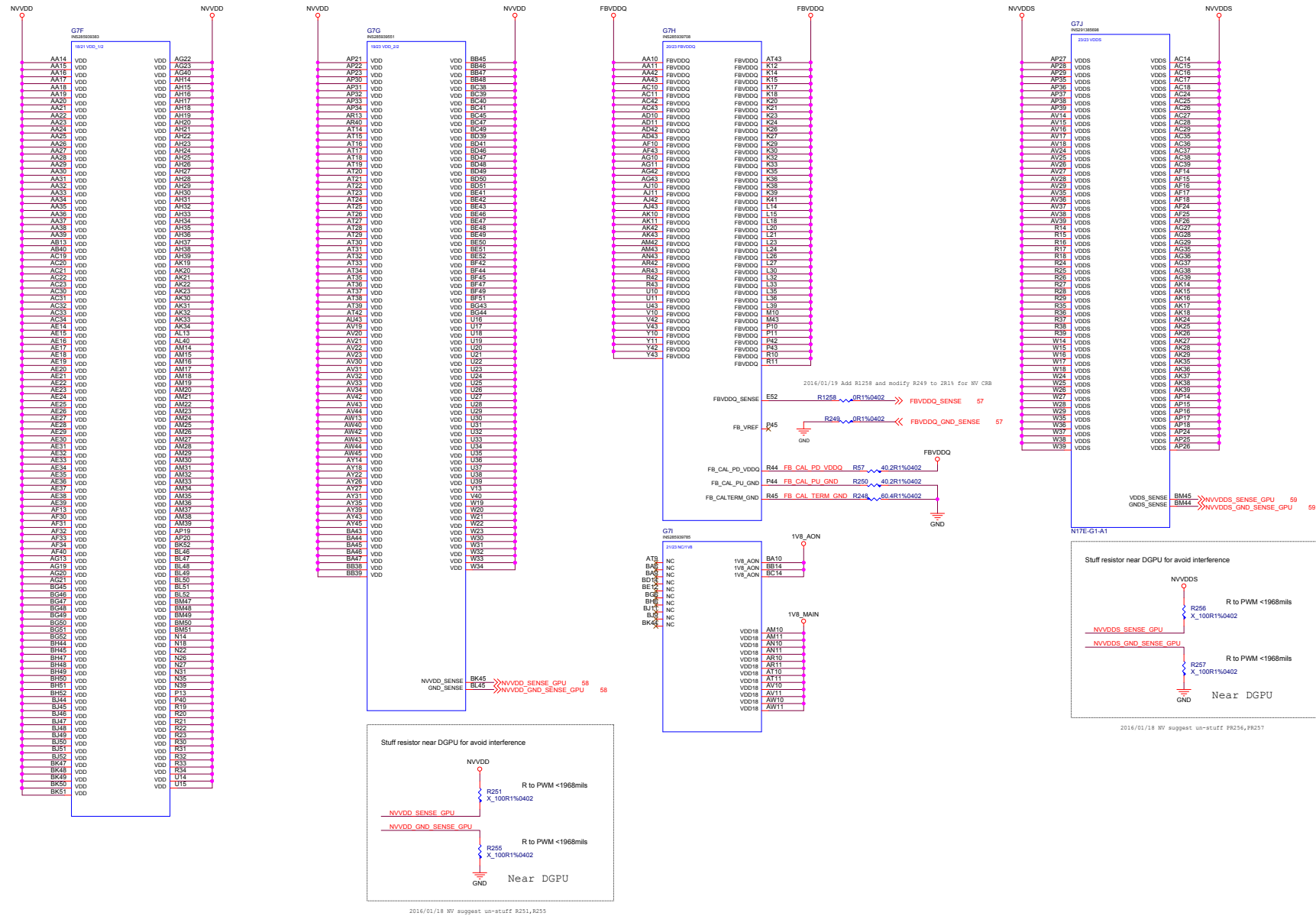
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alerts	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V <sup>2</sup>	SamSung	K4G0325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production candidate
			Hynix	H5GQ8H24MJR-R4C	W-die	0x2	8 Gbps	N/A	Full	Post production candidate

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

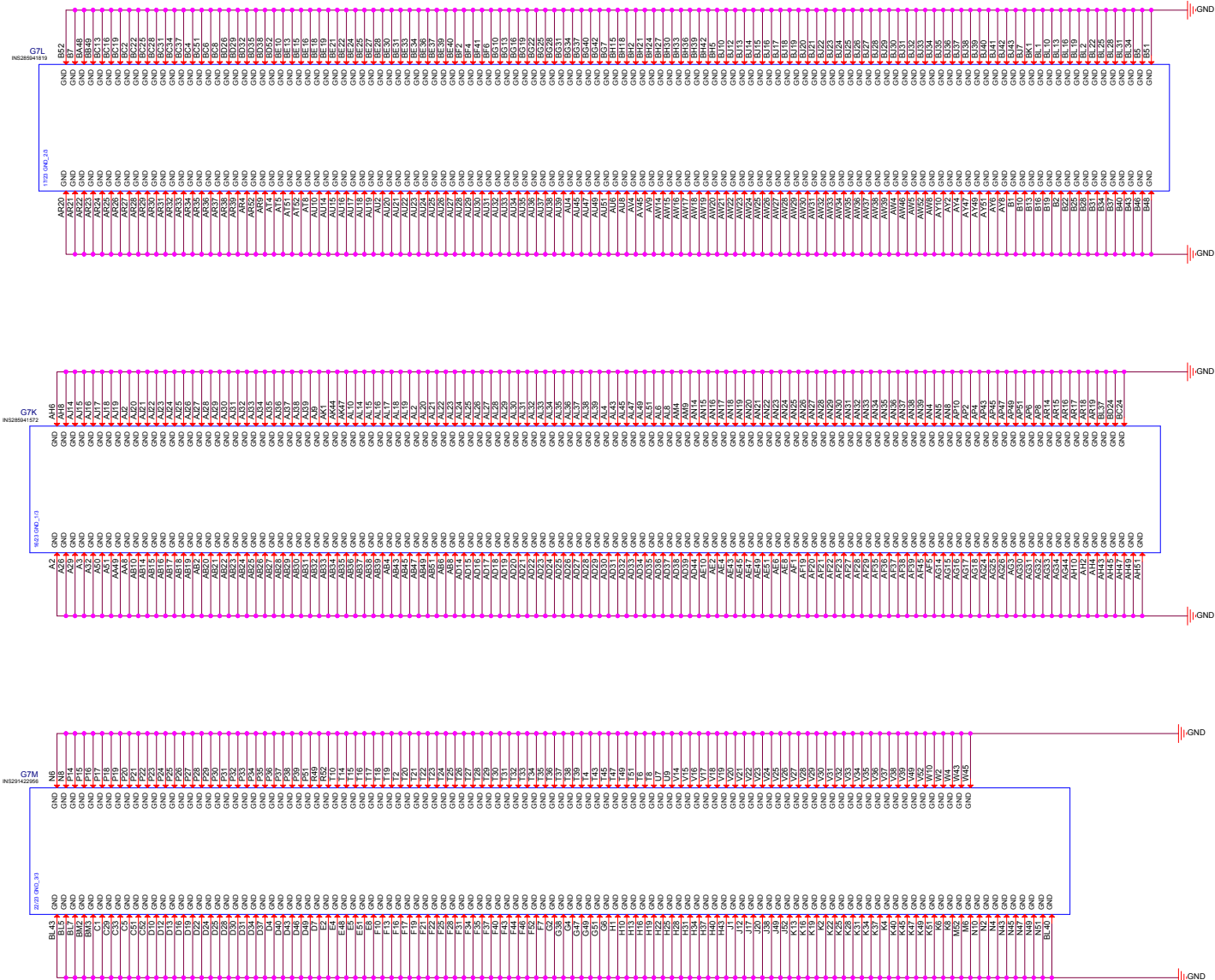
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE



## GPU NVVDD, FBVDDQ

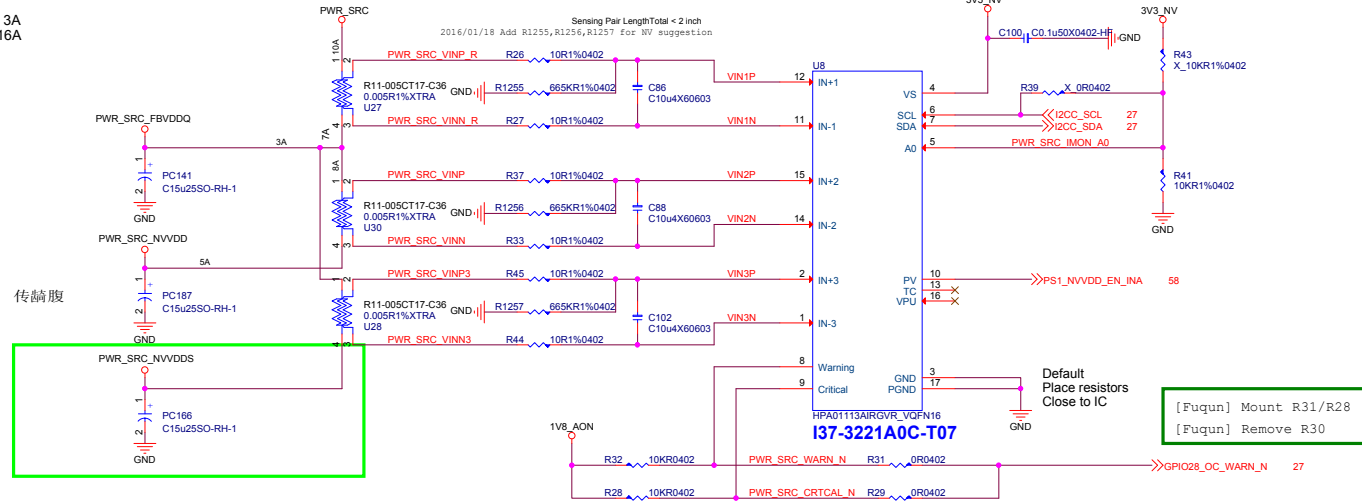


# DGPU GND

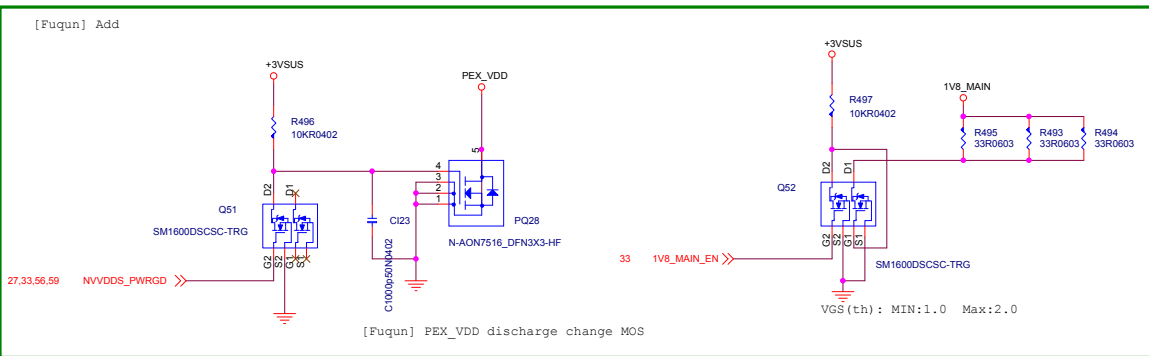
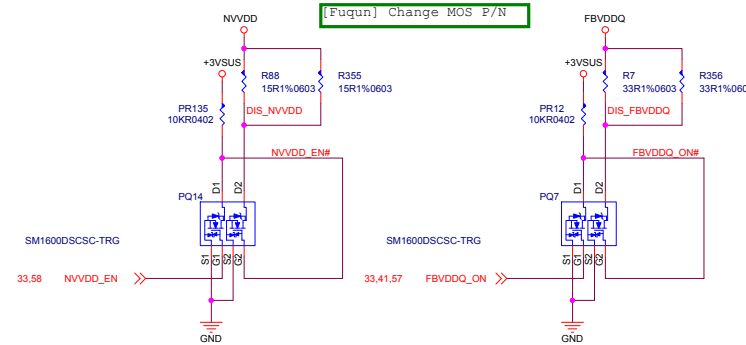
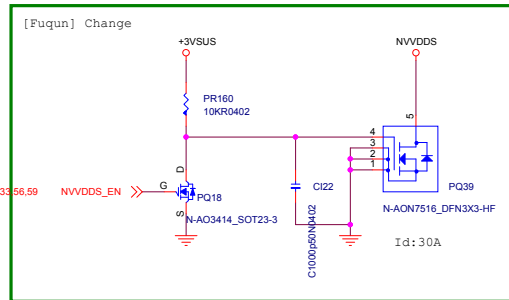


EDP Design Guide:  
N17E-G1(90W)  
NVVDD : 58A ; Peak 136A  
NVVDDS : 28A ; Peak 74A  
1.8V : 0.9A  
PEX\_VDD : 3A  
FBVDDQ : 16A

## DGPU\_Power Control



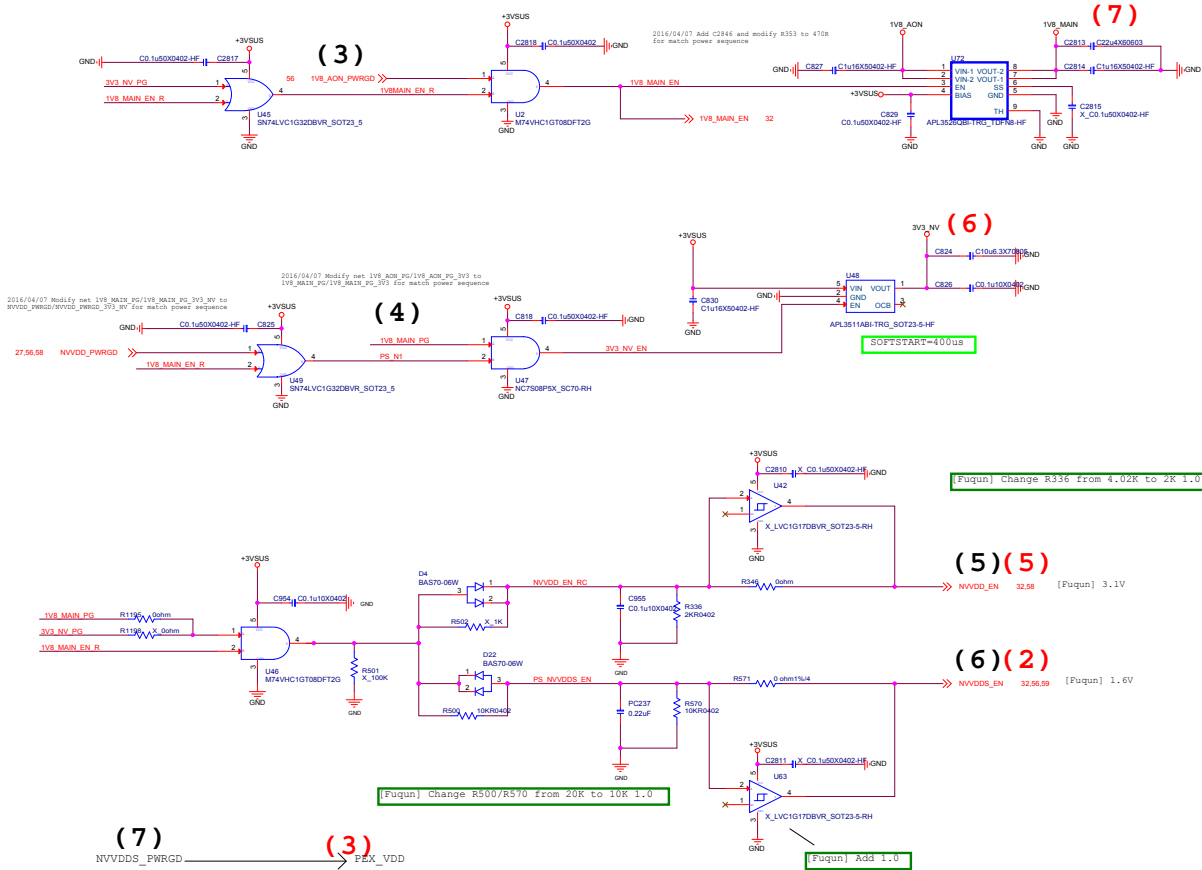
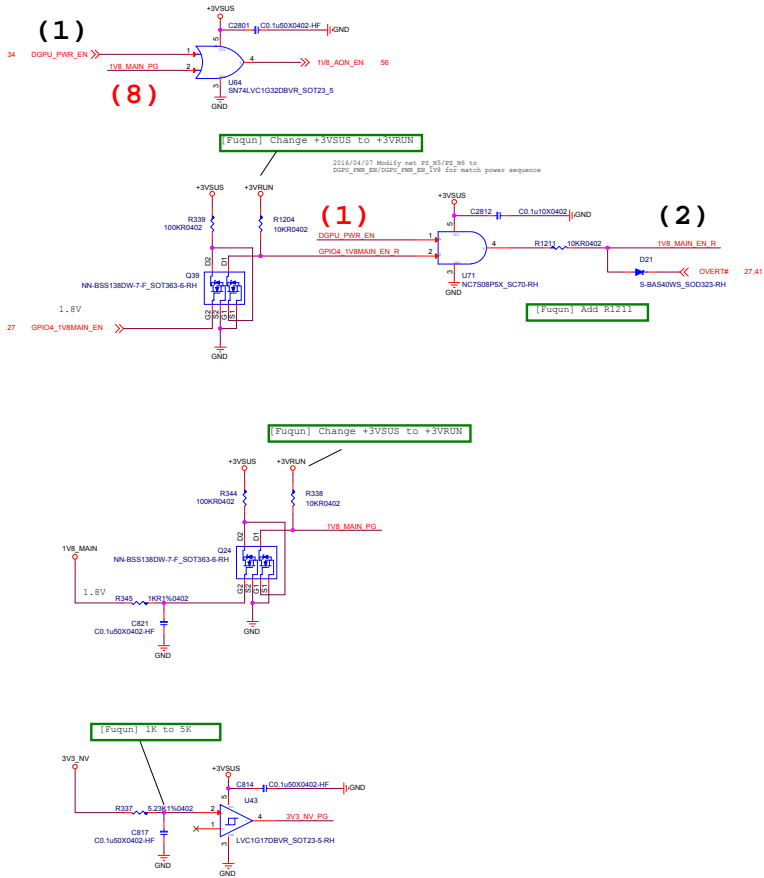
## Discharge



msi MICRO-STAR INT'L CO.,LTD.			
Title	DGPU Power control, Discharge		
Size	Document Number	Rev	
	MS-16JB1	0A	
Date	Sheet	32	of 71

nVIDIA Power Sequence Control

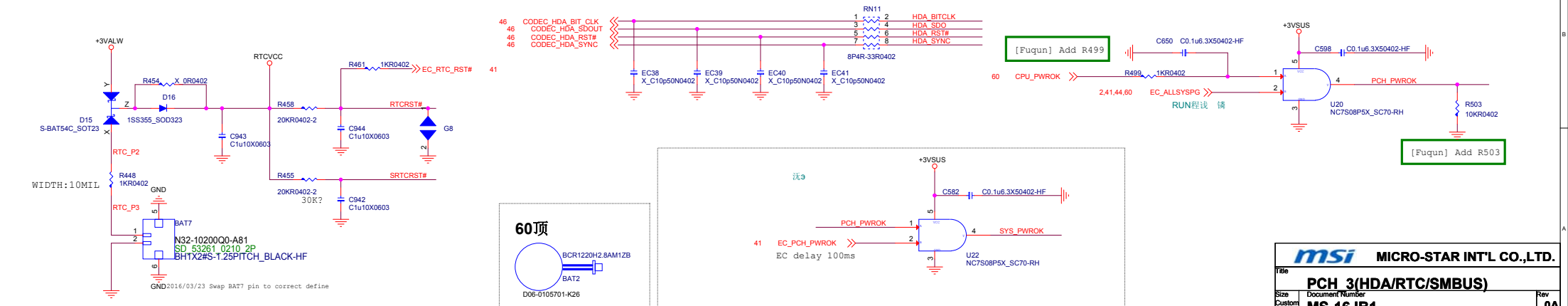
Power on = 1V8\_AON -> 1V8\_MAIN -> 3V3\_NV/NVDD -> NVDD/PEX\_VDD -> FBVDDQ -> DGPUPWRGD  
Power down = NVDD -> PEX\_VDD -> NVDD/FBVDDQ -> 3V3\_NV -> 1V8\_MAIN -> 1V8\_AON







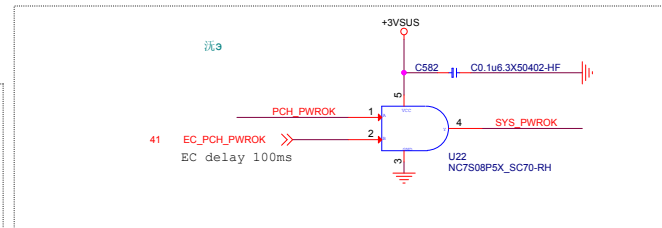
PCH EDS Page 52




BCR1220H2.8AM1ZB

BAT2

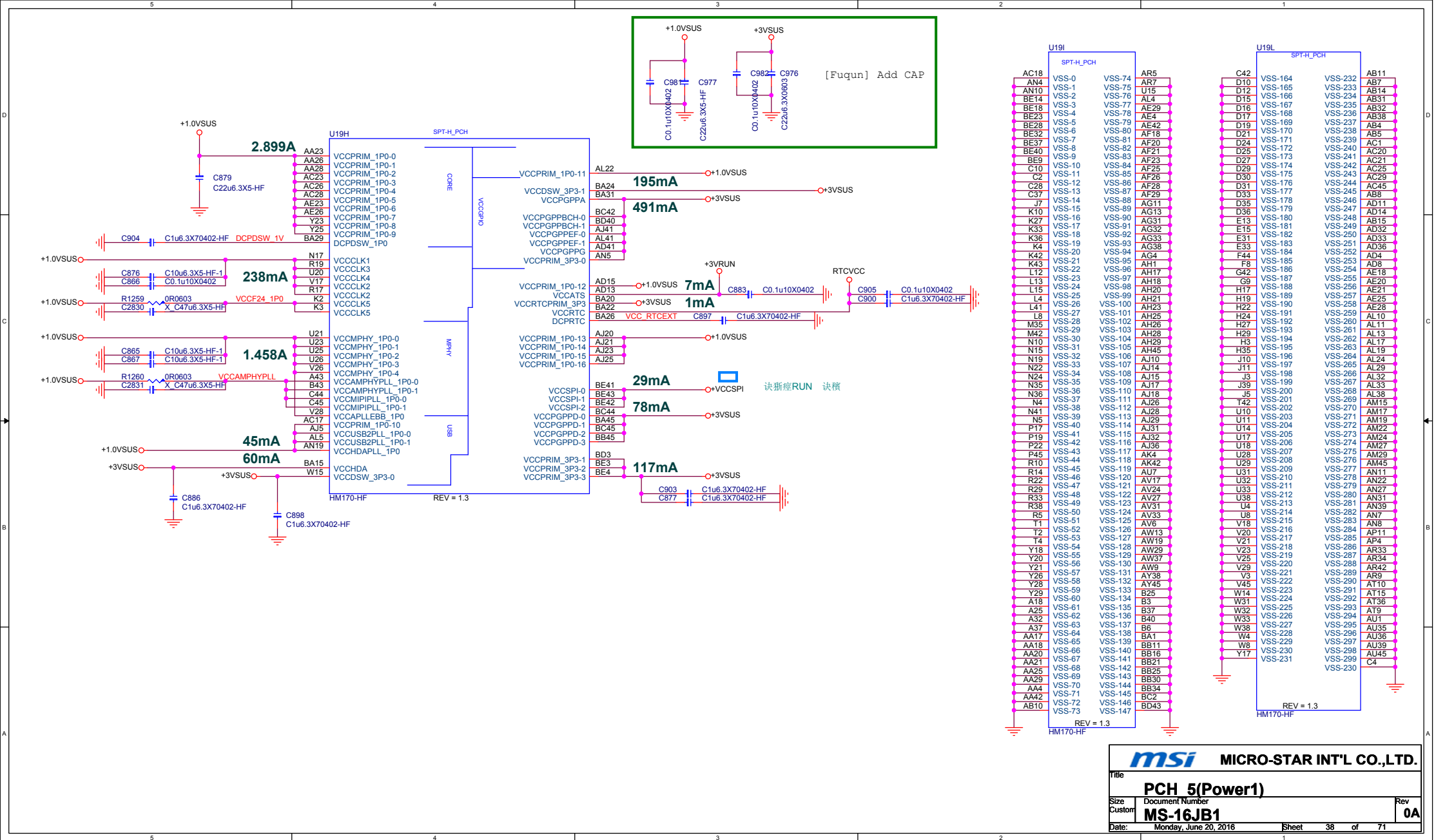
D06-0105701-K26



 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>PCH 3(HDA/RTC/SMBUS)</b>	
Size	Document Number
Custom	<b>MS-16JB1</b>
Date:	Monday, June 20, 2016
Sheet	36 of 71
Rev	<b>0A</b>



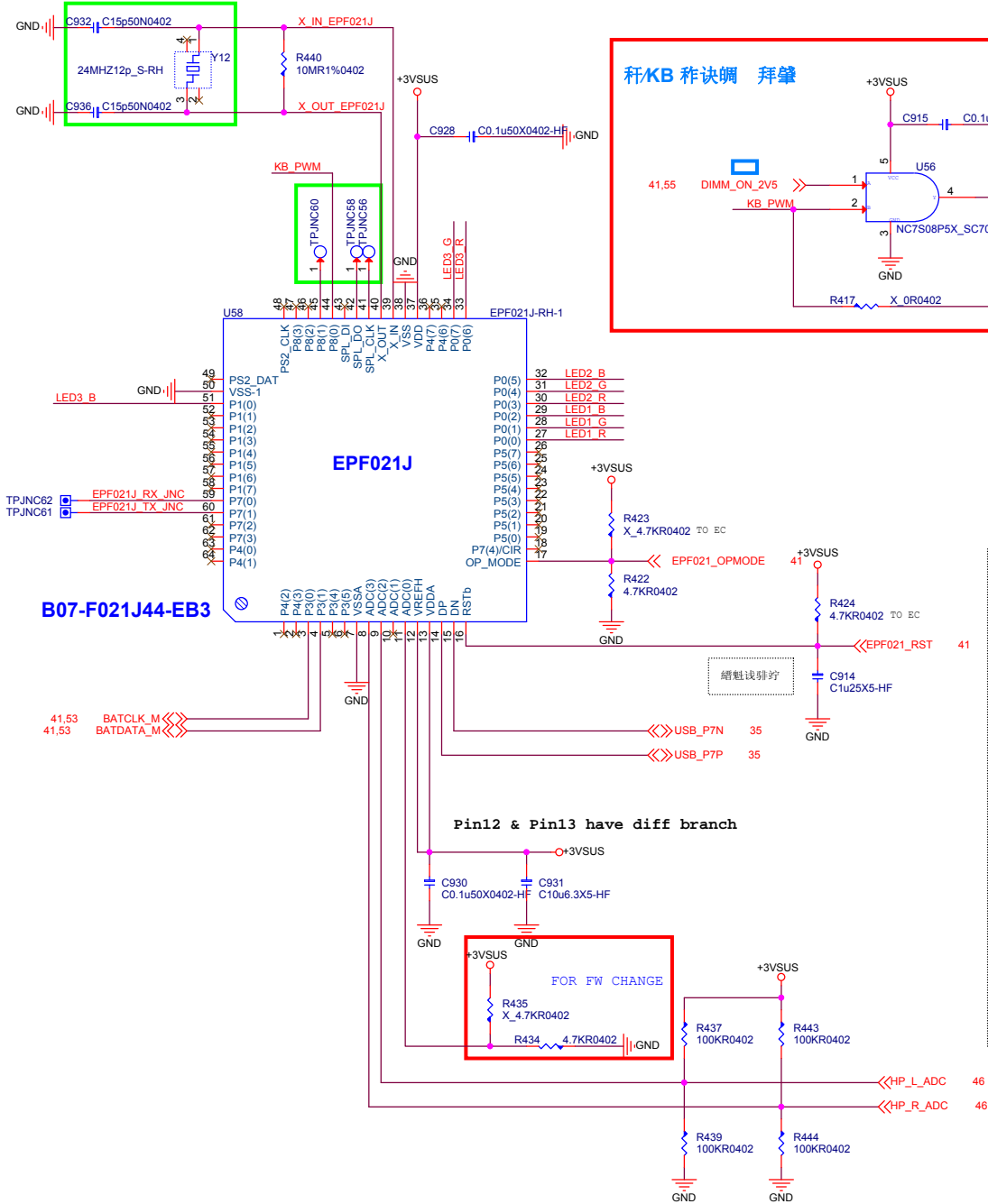




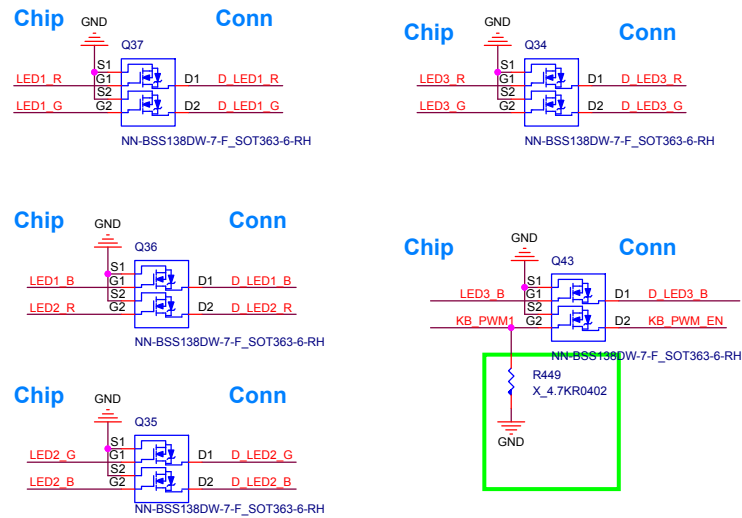


LED 8051 Controller

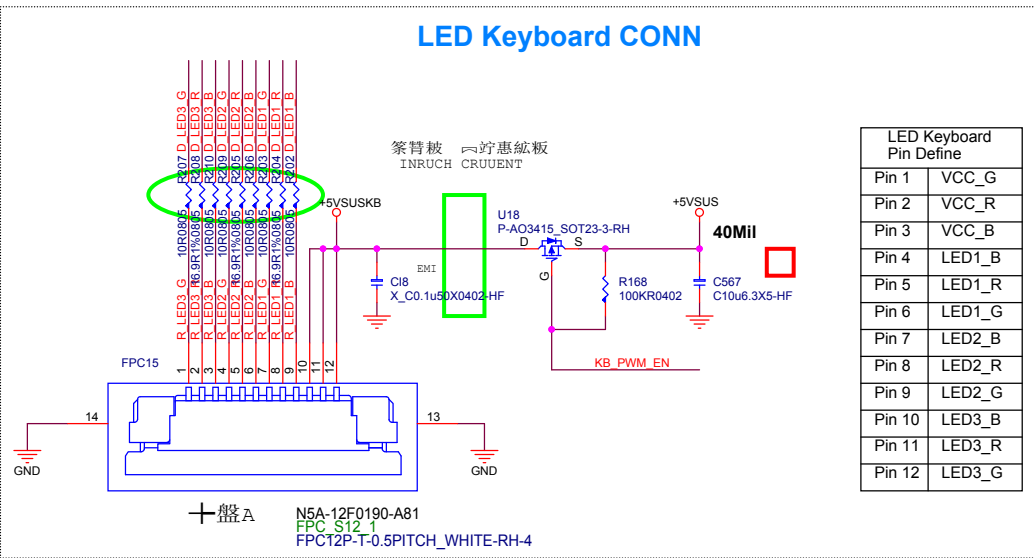
C749 and C750 change to 15pF for SA



EPF021J Sink current not enough, only using BSS138 (0.22A)

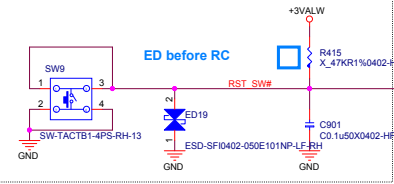


LED Keyboard CONN



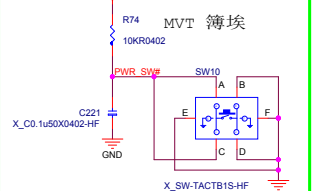
# KBC/EC/uP (ENE9028)

## Hardware Reset

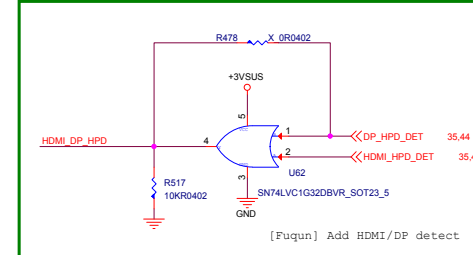


[Fuqun] Remove LPC debug

## HW Debug

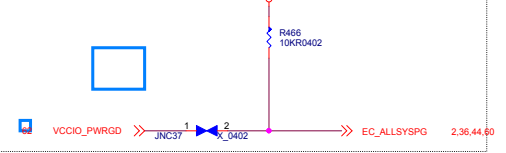


[Fuqun] Remove 1.0

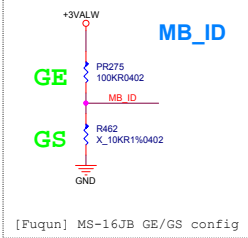
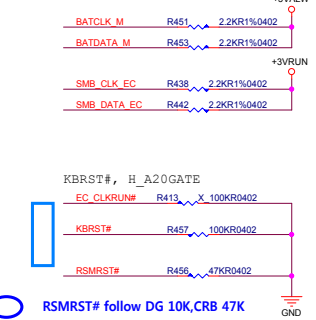


[Fuqun] Add HDMI/DP detect

## ALLSYSPG

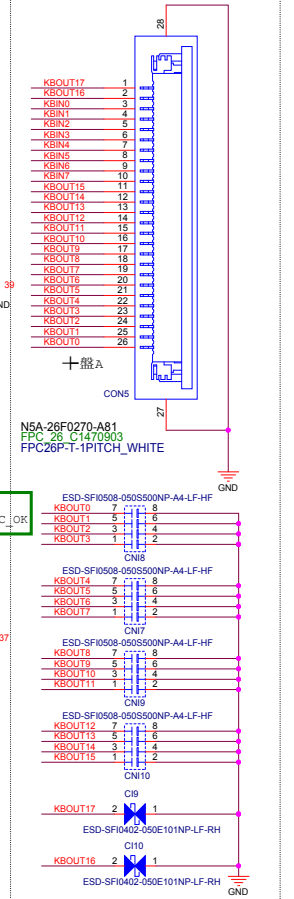


## PU/PD

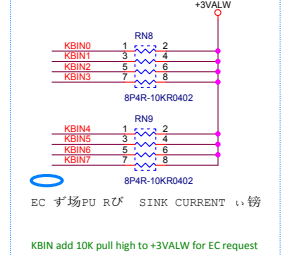


[Fuqun] MS-16JB GE/GS config

## Keyboard conn



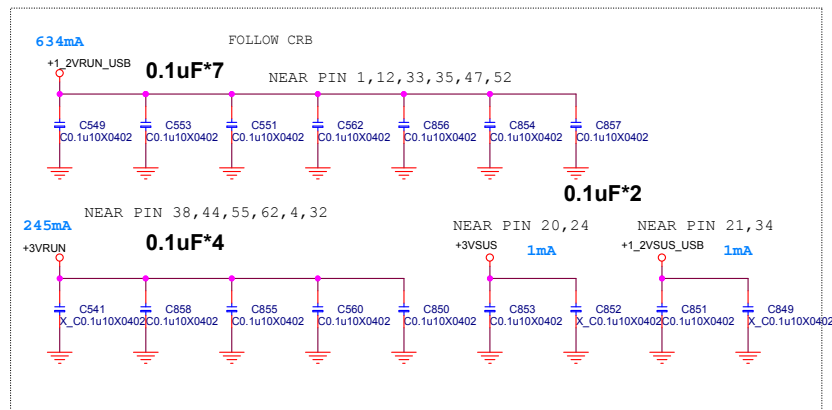
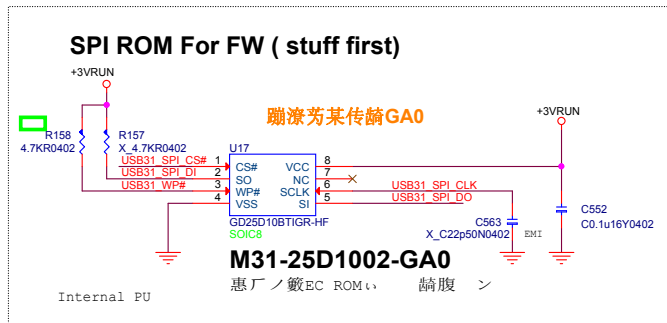
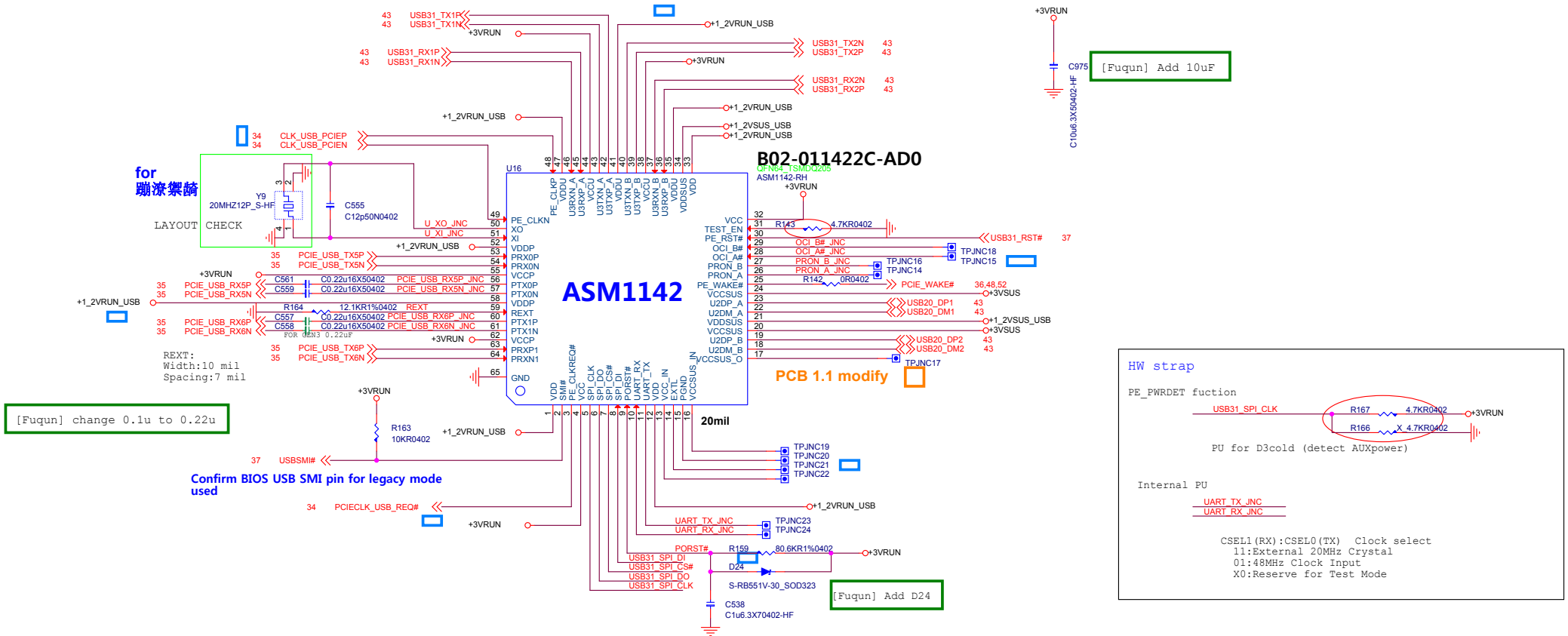
2016/04/22 Modify C19, C110 to 00G-0402500-B10 and CN17, CN18, CN19, CN110 to 00G-5000S10-B10 for DM request



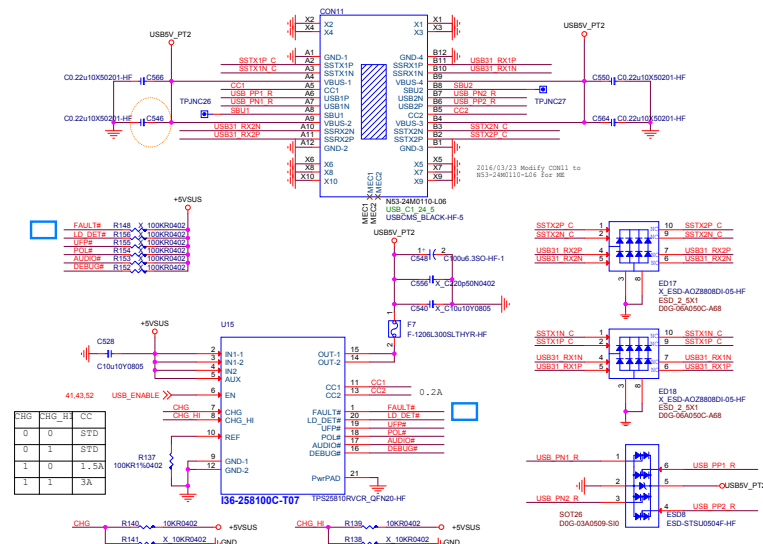
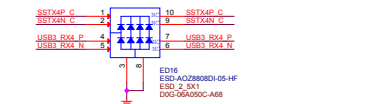
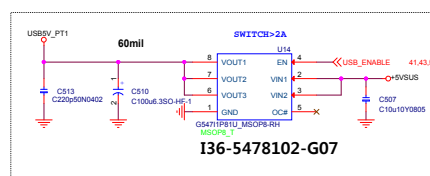
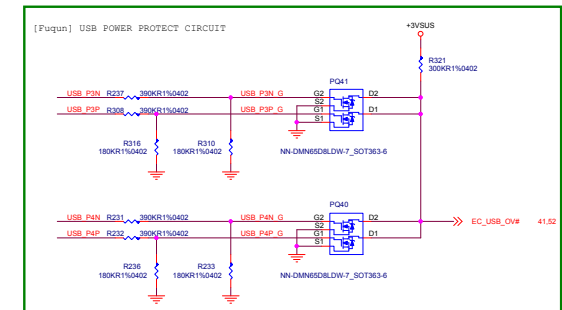
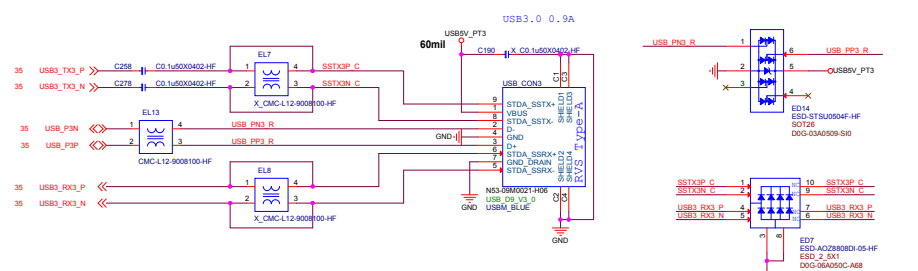
KBIN add 10k pull high to +3VALW for EC request

# PCIE to USB 3.1

USB 3.0/  
USB 3.1

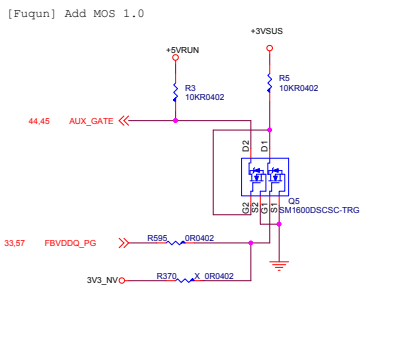
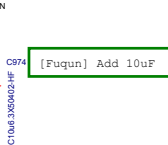
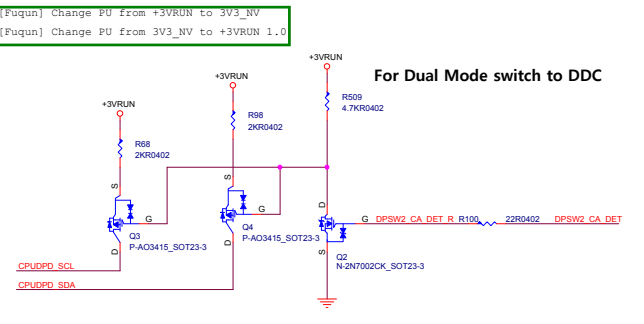
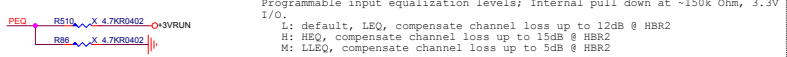
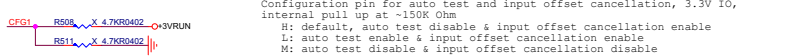
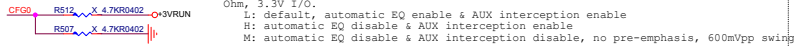
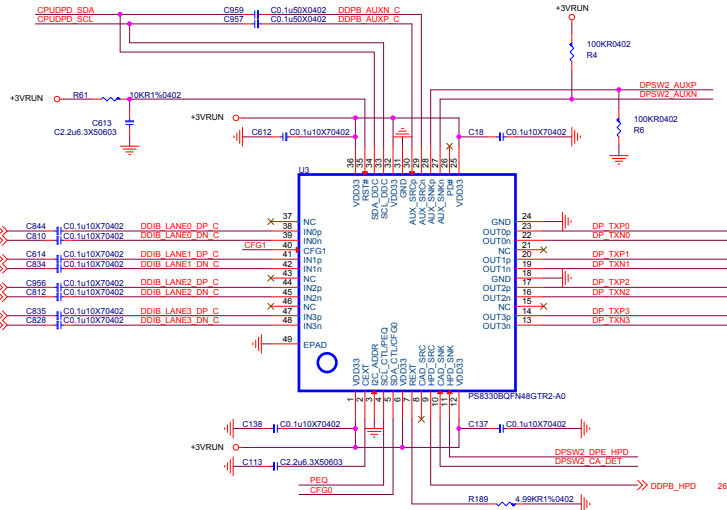
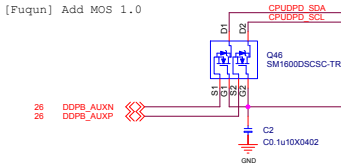




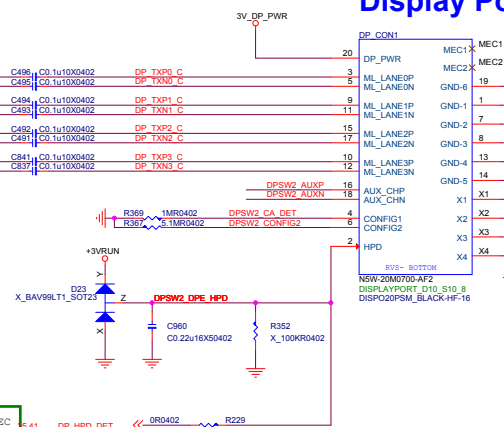
[illegible][illegible]



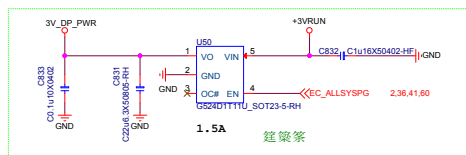
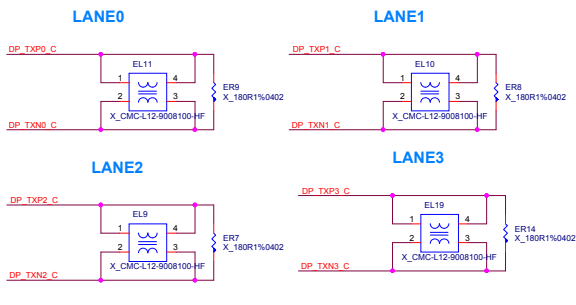
[Fugun] Add level shift



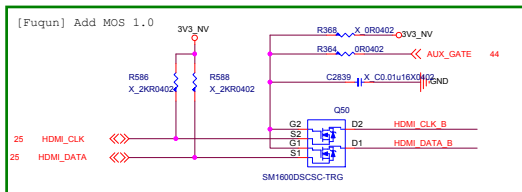
## Display Port



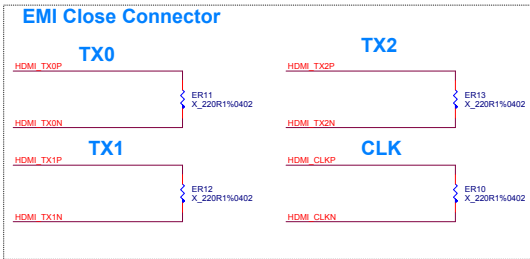
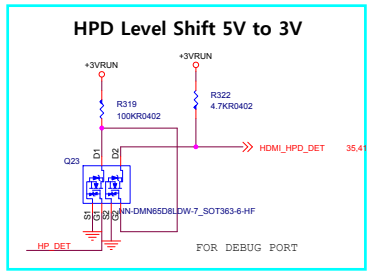
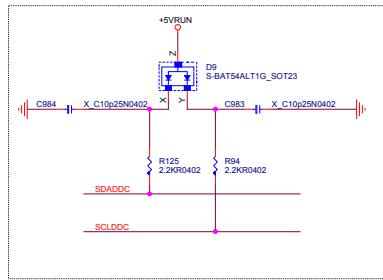
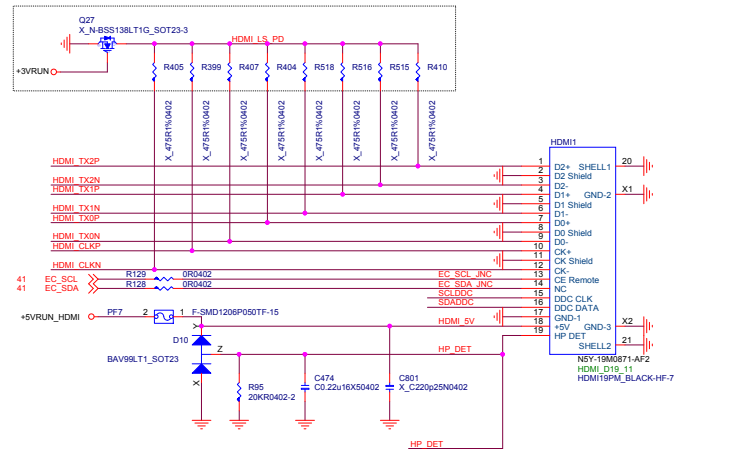
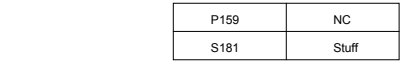
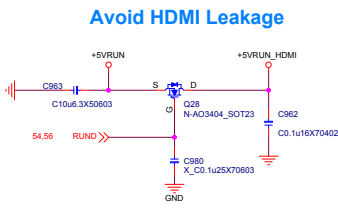
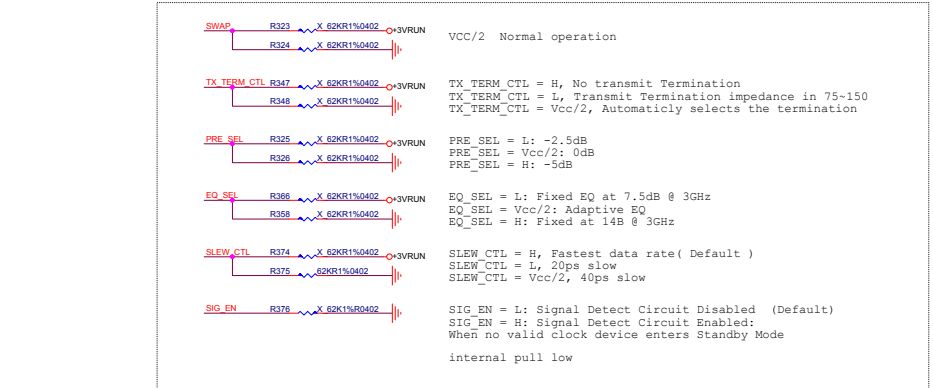
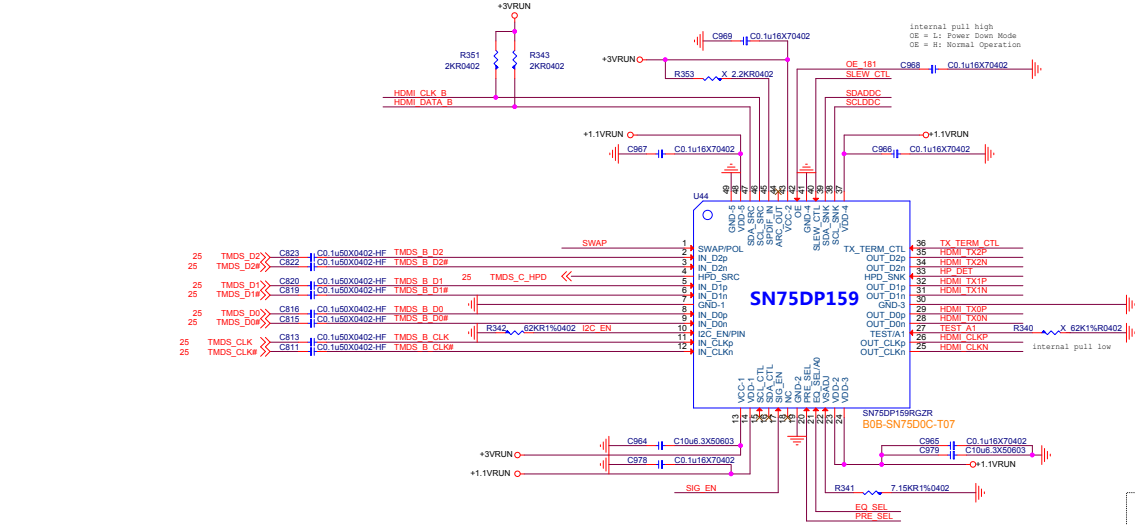
## EMI Close Connector



## HDMI Level Shifter

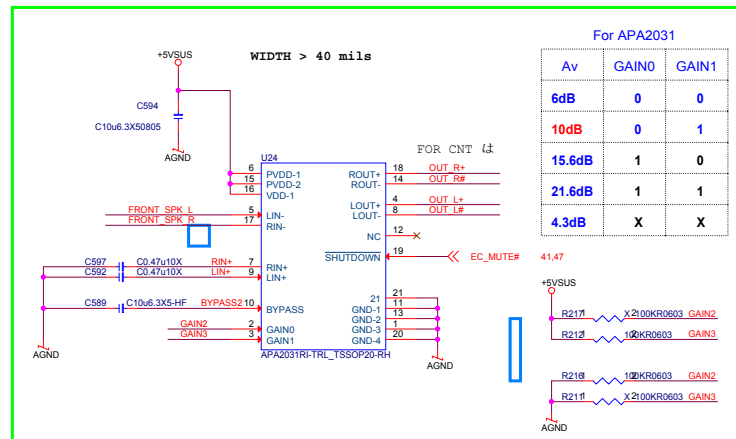
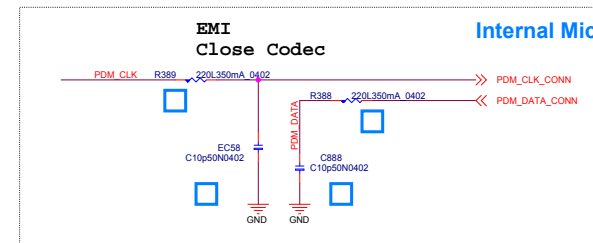
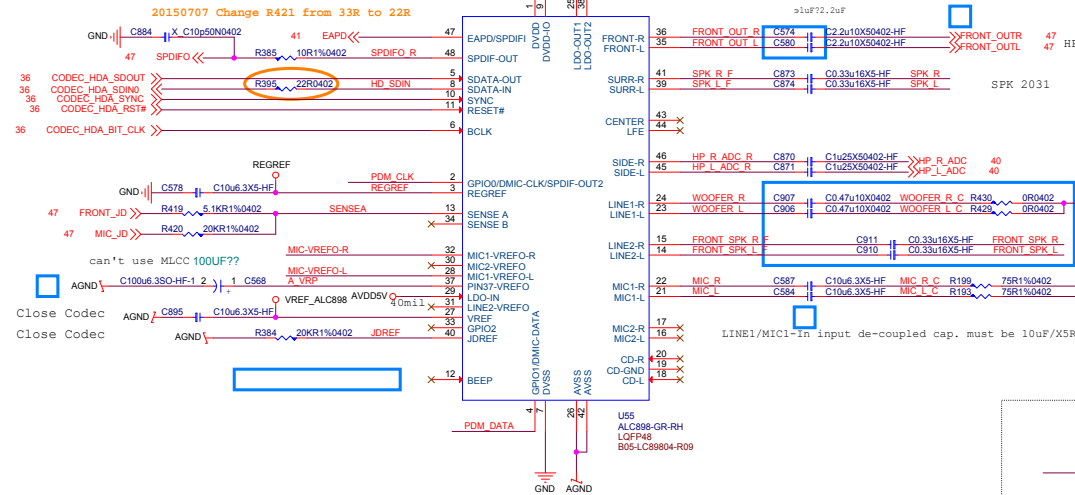
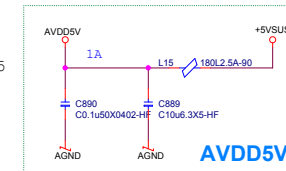
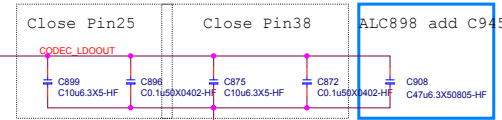
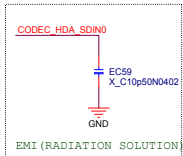
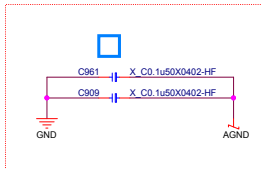


```
[Fuqun] Change +3VRUN to 3V3_NV
[Fuqun] Change NV_3V3 to 3VRUN 1.0
```

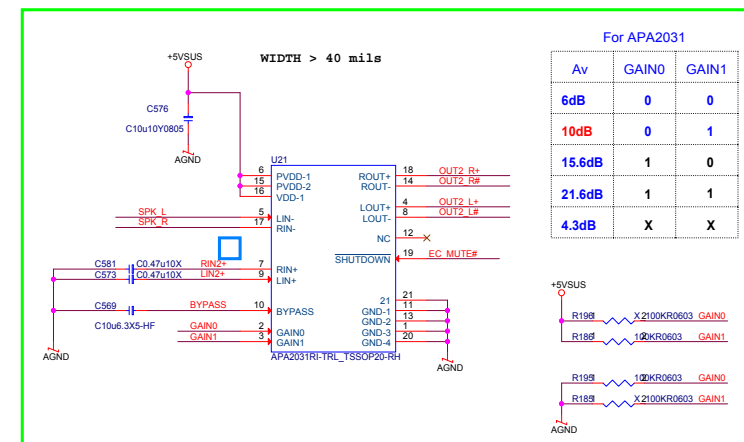


閣MOAT 策瑞+ COOPER

閣MOAT 策瑞+ COOPER



Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

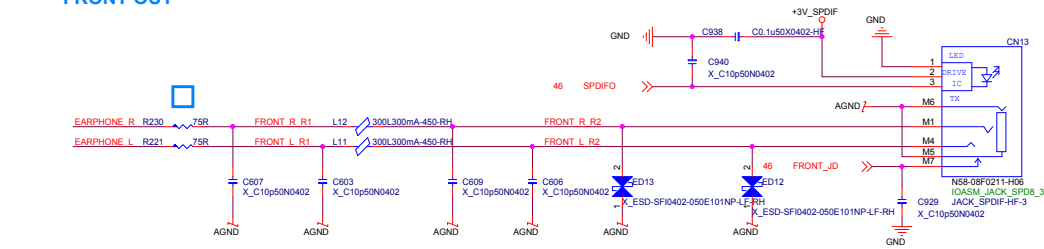


Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

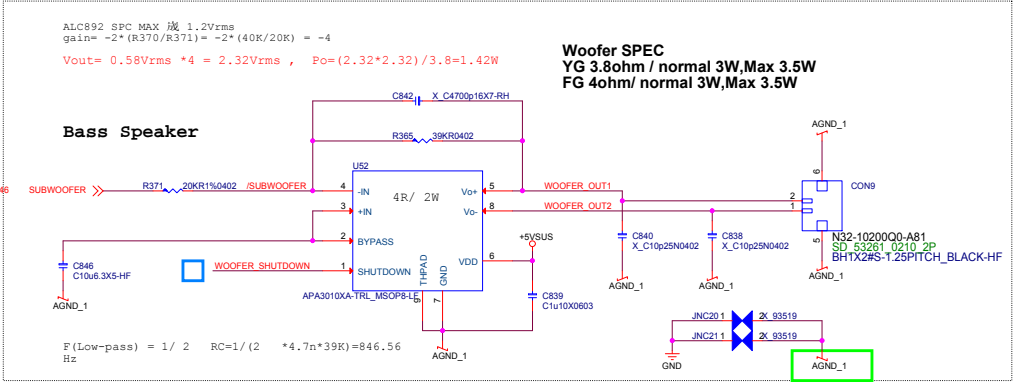
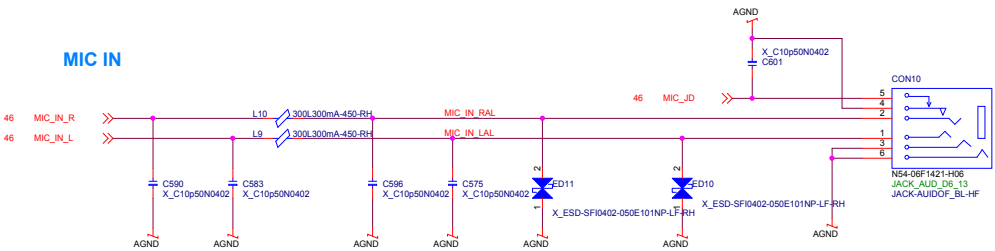
	CODEC	斥
L	-	-
L	+	+
R	+	+
R	-	-
L2	+	+
L2	-	-
R2	-	-
R2	+	+

Audio CONN /Woffler

FRONT OUT



MIC IN

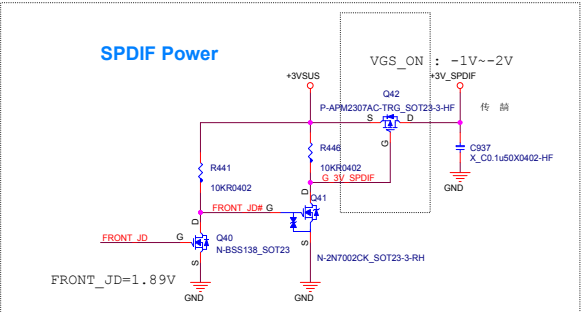


Woofer SPEC  
YG 3.8ohm / normal 3W,Max 3.5W  
FG 4ohm/ normal 3W,Max 3.5W

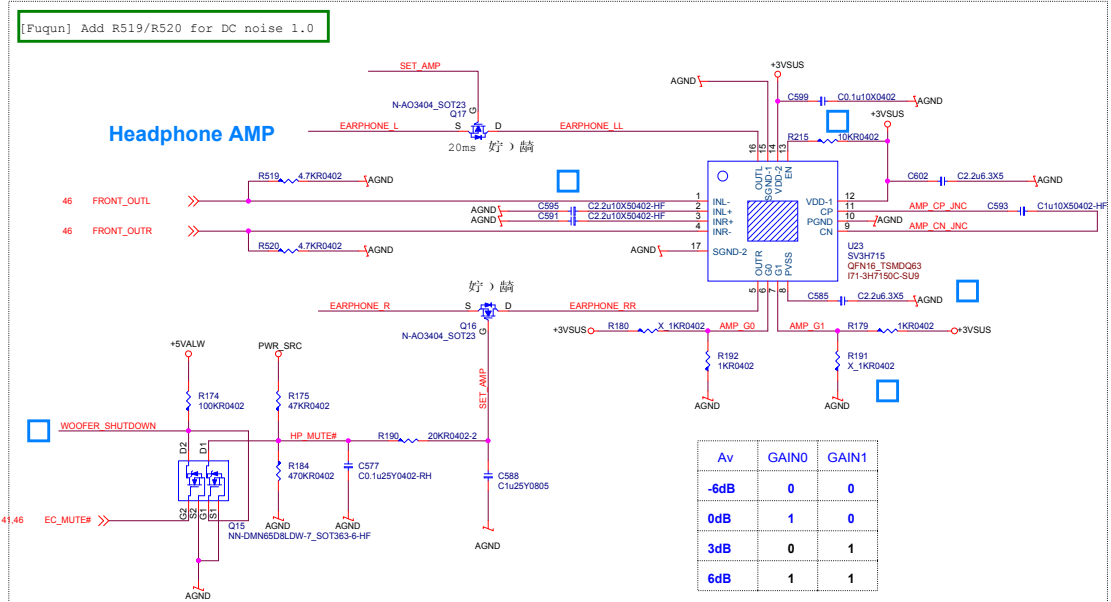
Bass Speaker

$$F(\text{Low-pass}) = \frac{1}{2} \quad RC = \frac{1}{(2 \times 4.7n \times 39K)} = 846.56 \text{ Hz}$$

SPDIF Power

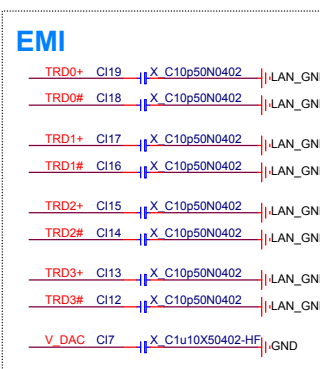
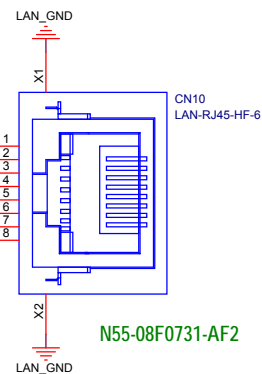
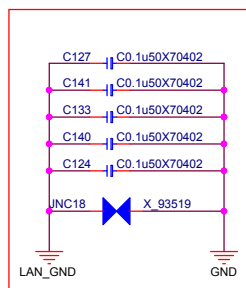
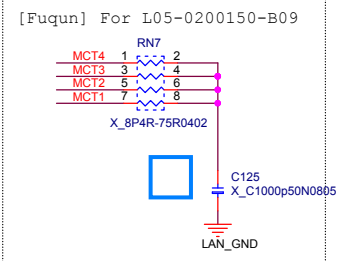
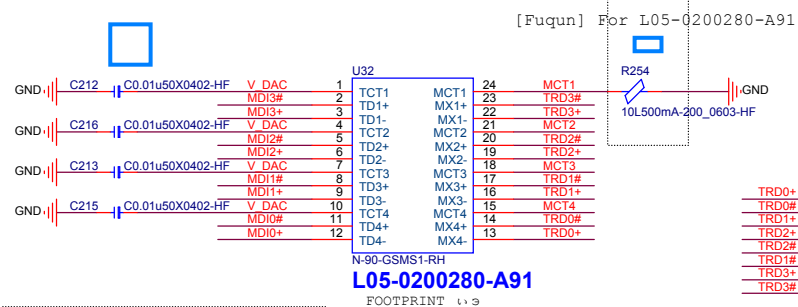
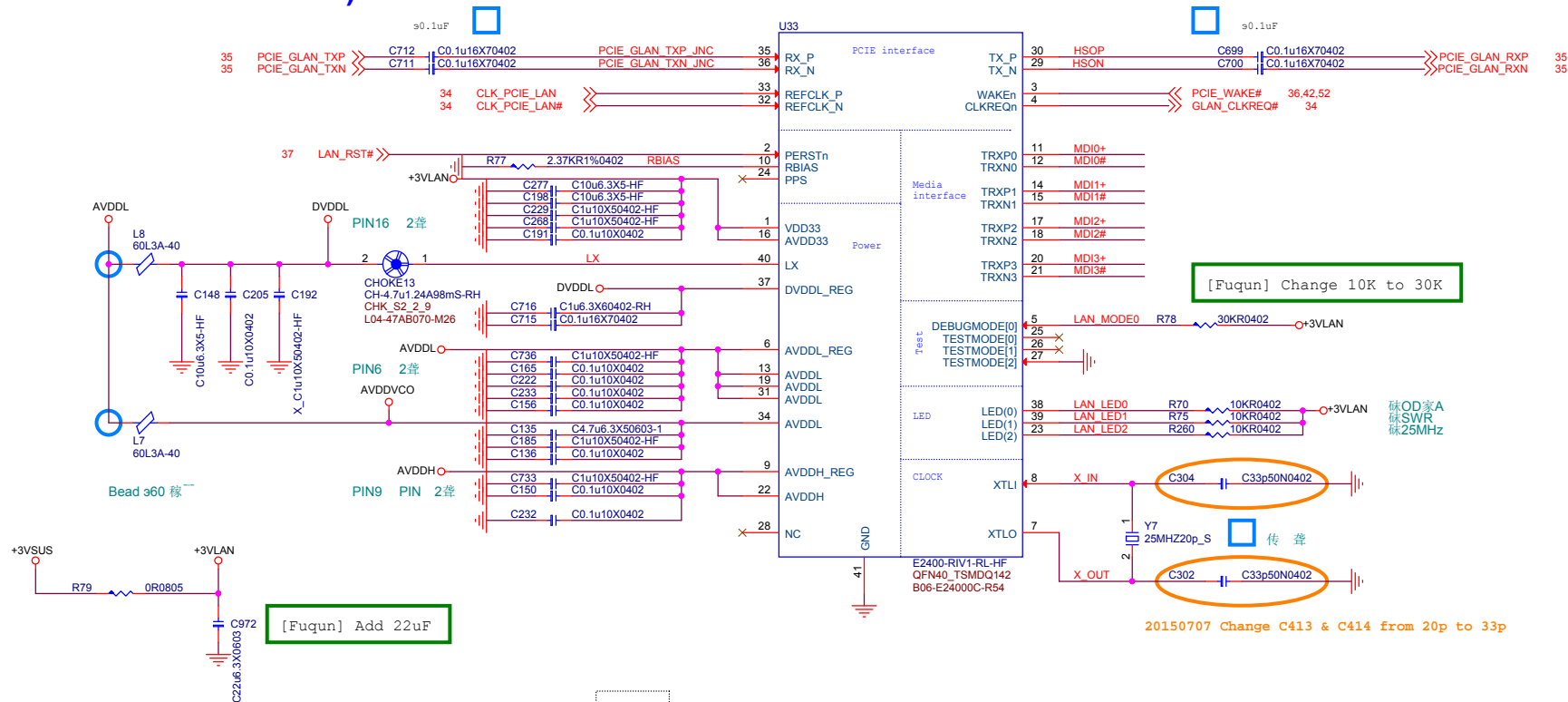


Headphone AMP

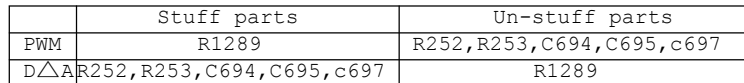


Av	GAIN0	GAIN1
-6dB	0	0
0dB	1	0
3dB	0	1
6dB	1	1

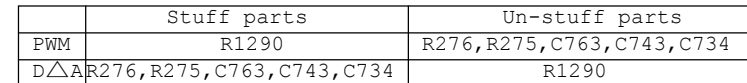
## GIGA LAN(BigFoot BFN2400B)



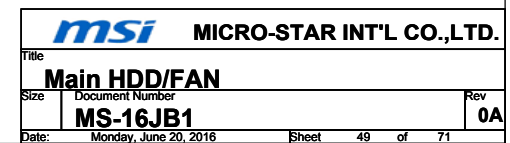
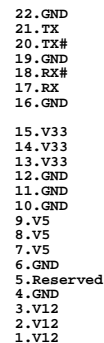
## [Fuqun] Remove IC



## [Fuqun] Remove IC

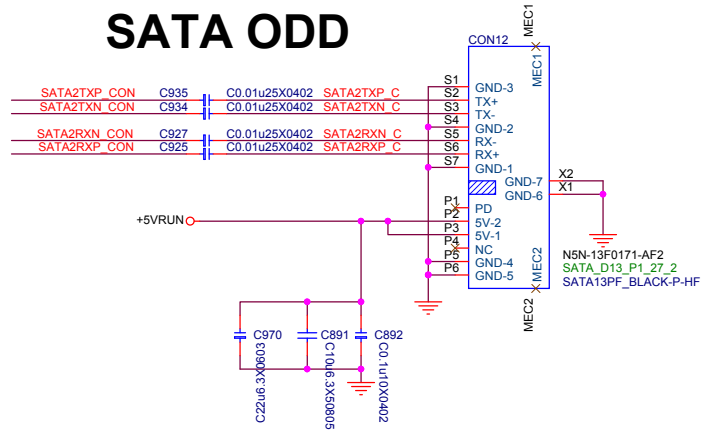


[Fuqun] For MS-16JB GE

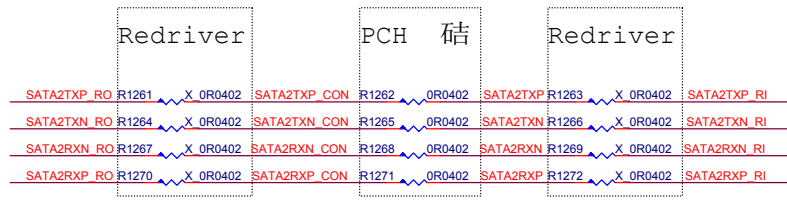
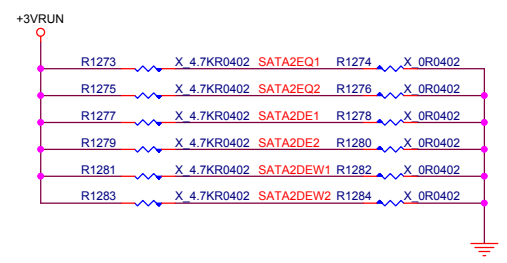




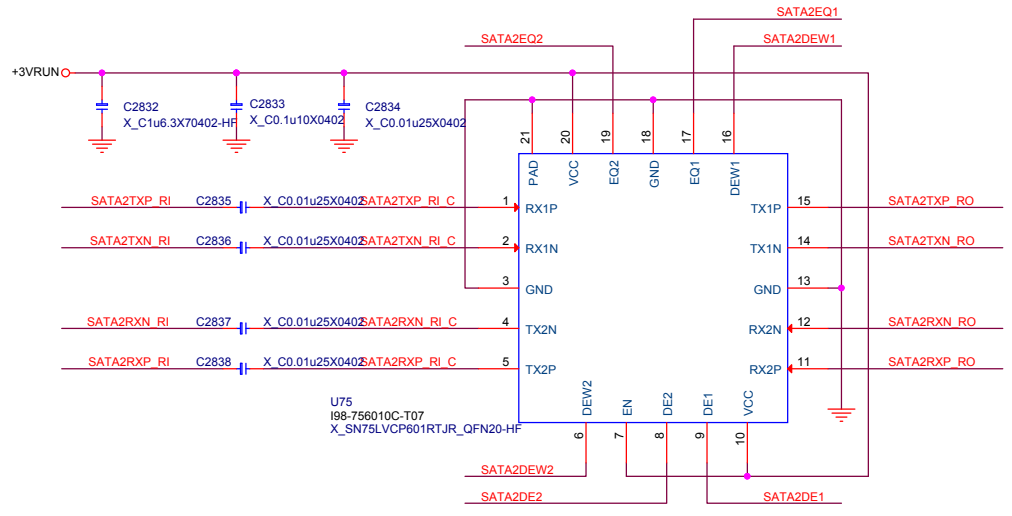
# SATA ODD



[Fuqun] Add 22uF



# Verge HDD reDRIVER

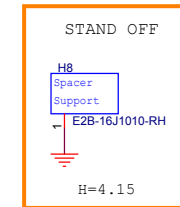
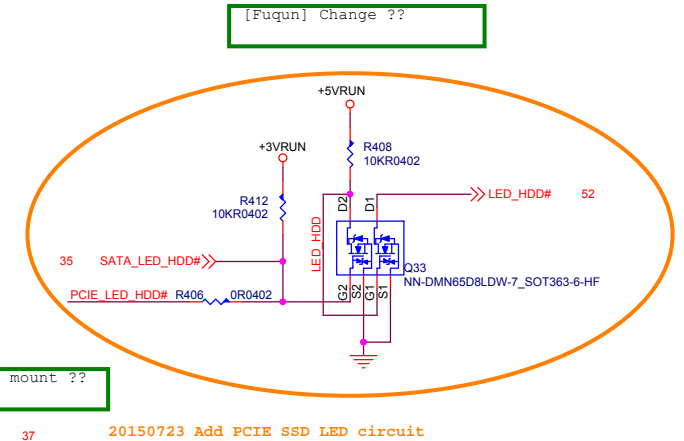
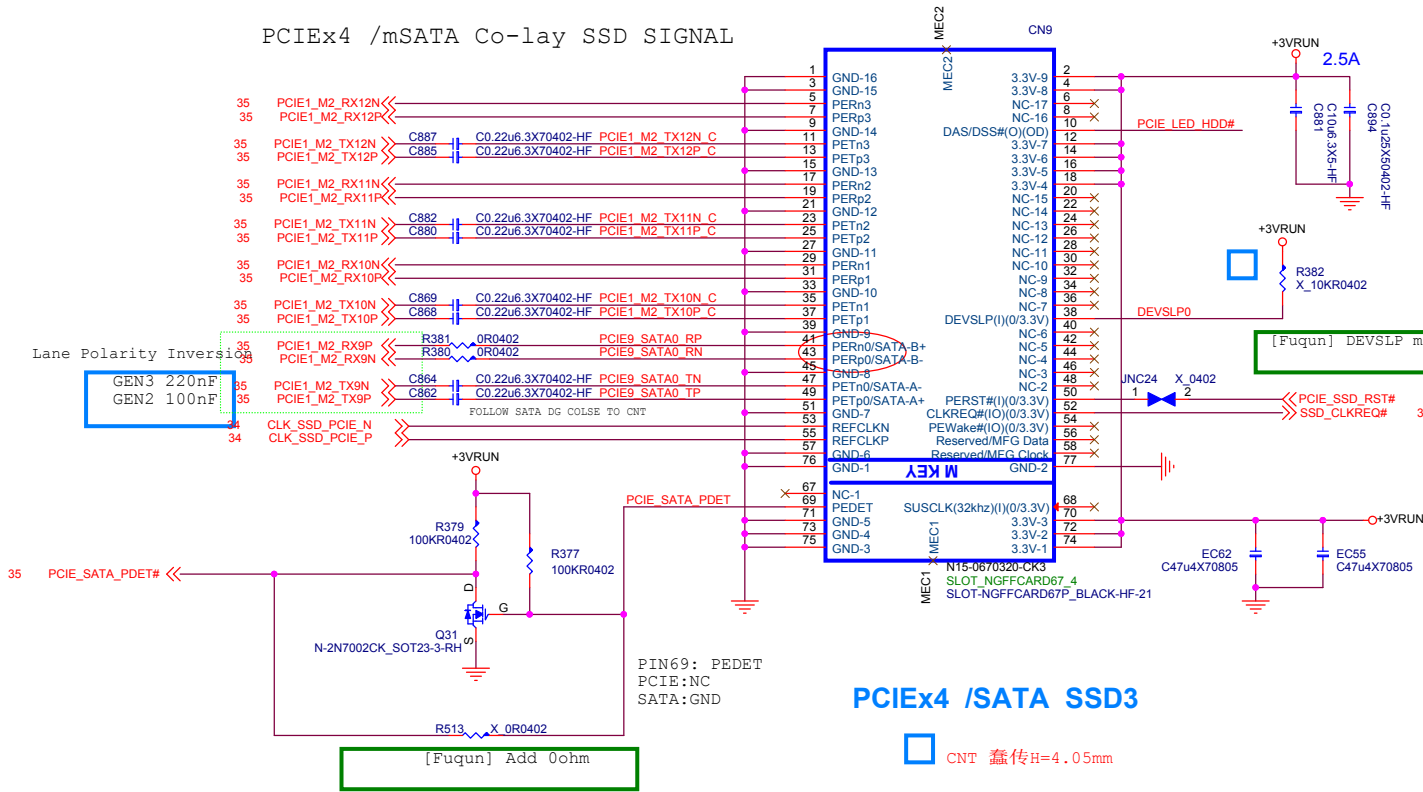


## TX and RX EQ and DE Pulse-Duration Settings

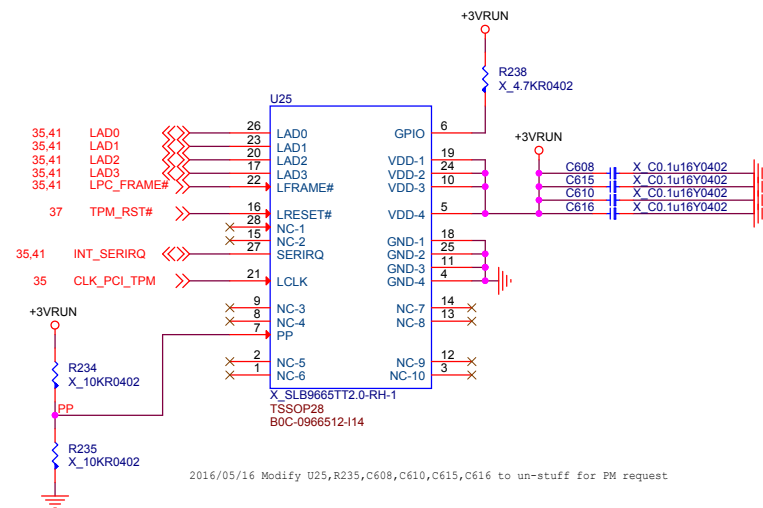
DE1 OR DE2	CH1 OR CH2 DE-EMPHASIS dB (at 6 Gbps)	EQ1 OR EQ2	CH1 OR CH2 Equalization dB (at 6 Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14
DEW1 OR DEW2	DEVICE FUNCTION → DE WIDTH FOR CH1/CH2		
0	De-emphasis pulse duration, short		
1 (default)	De-emphasis pulse duration, long		



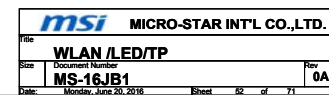
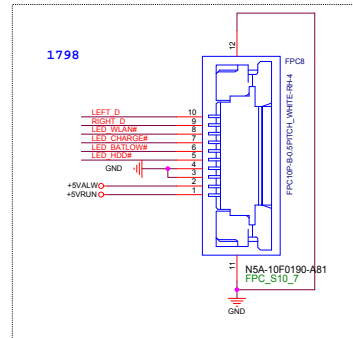
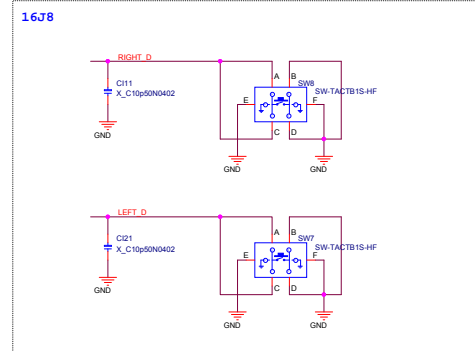
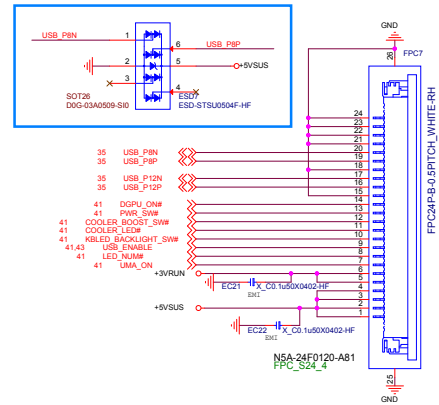
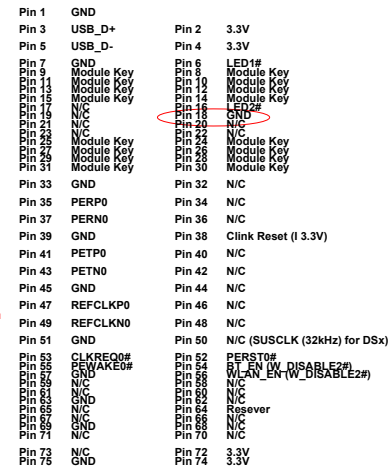
# PCIEx4 /mSATA Co-lay SSD SIGNAL



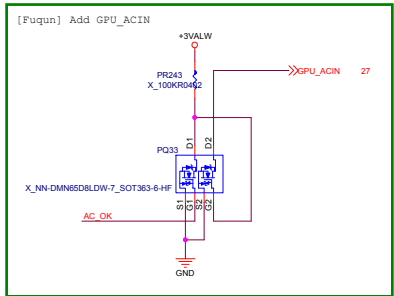
## TPM



## WLAN/LED

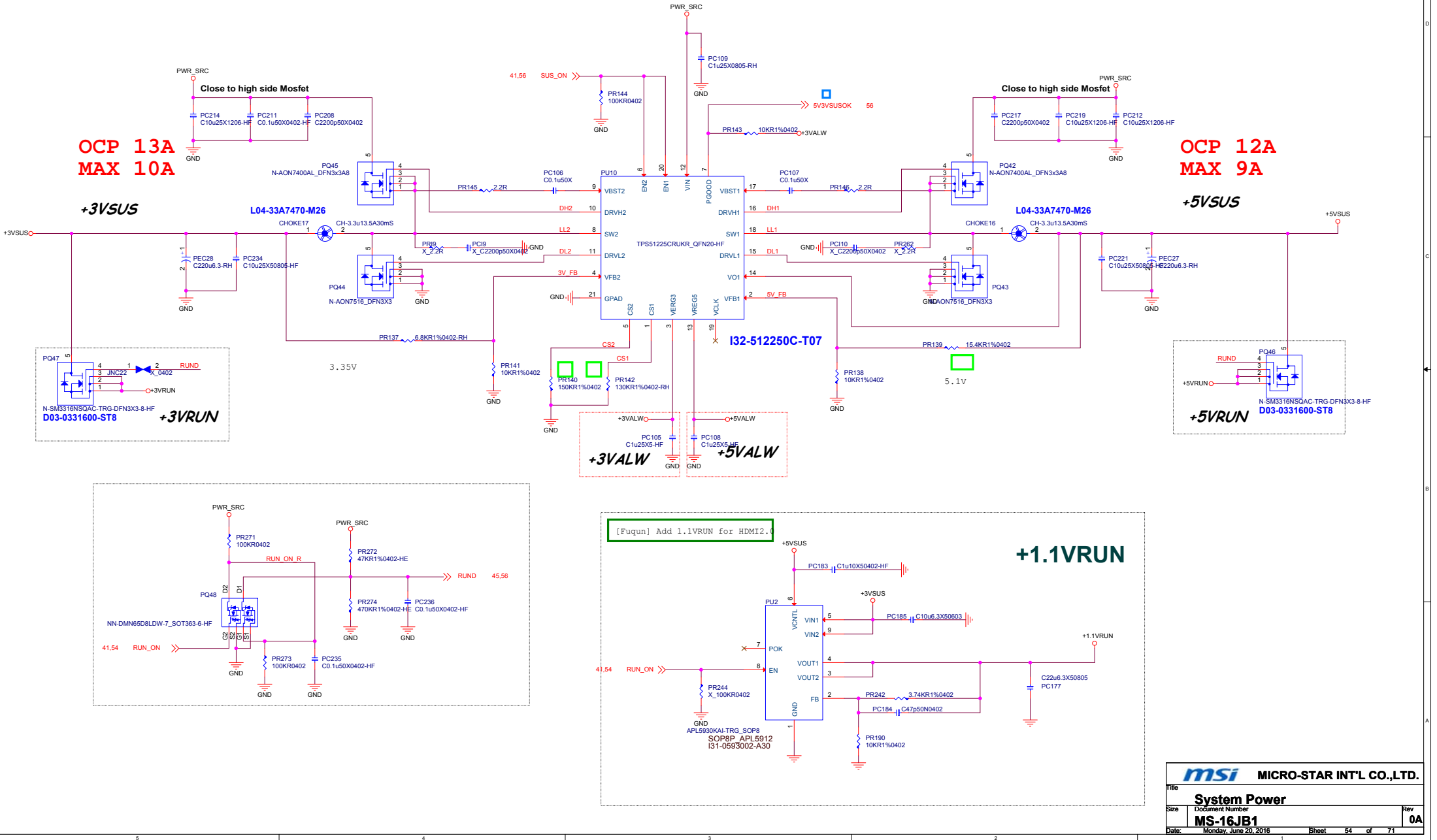


## Battery Select



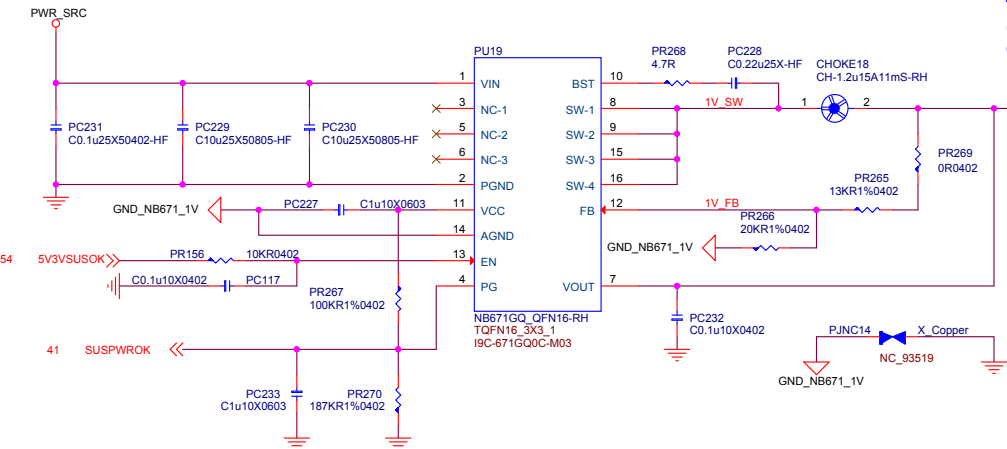
# System Power

[Fuqun] Change CHOKE16/17 from 33A7400 to 33A7470 1.0





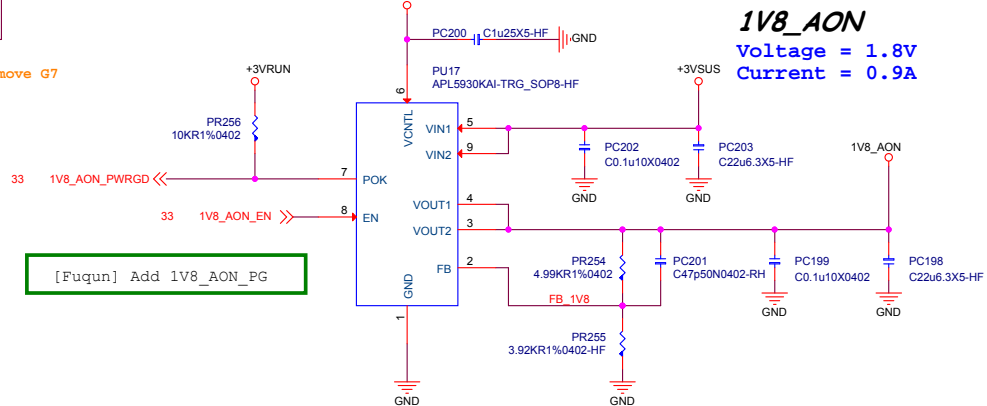
# +1VSUS



# +1.0VSUS

Voltage = 1V  
Current = 5A  
OCP(typi) = 8A

+1.0VSUS



# 1V8\_AON

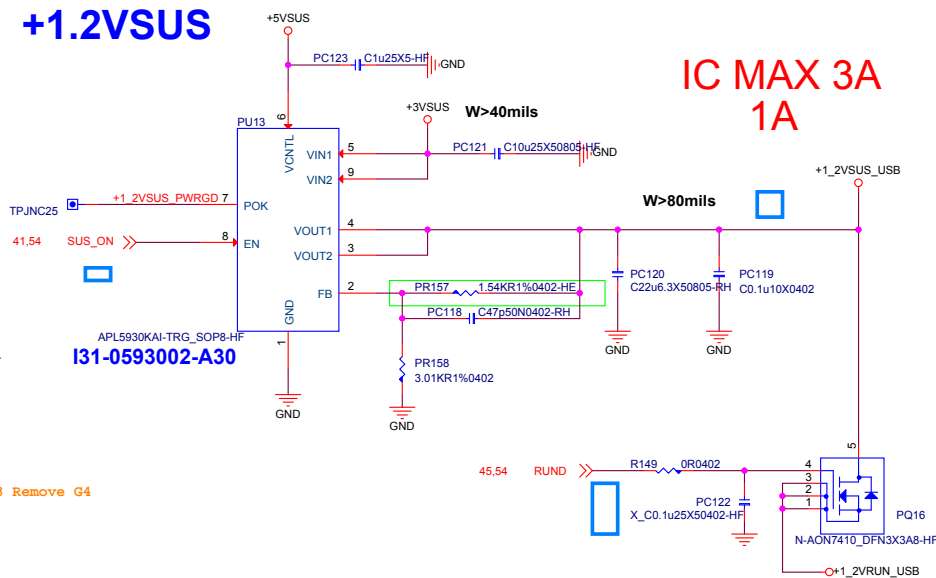
Voltage = 1.8V  
Current = 0.9A

1V8\_AON

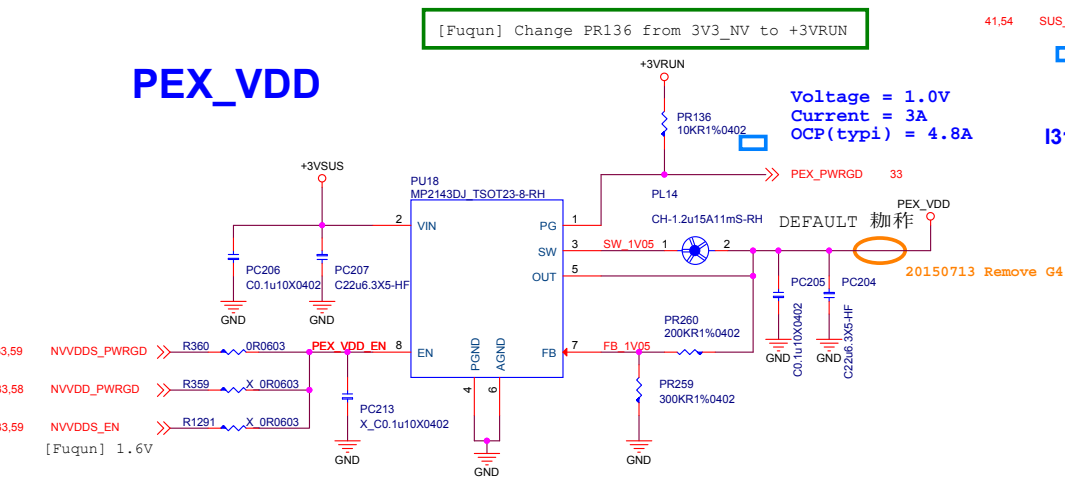
2016/02/17 Modify PR255 3.92Kohm for Power suggestion

# +1.2VSUS

IC MAX 3A  
1A



# PEX\_VDD



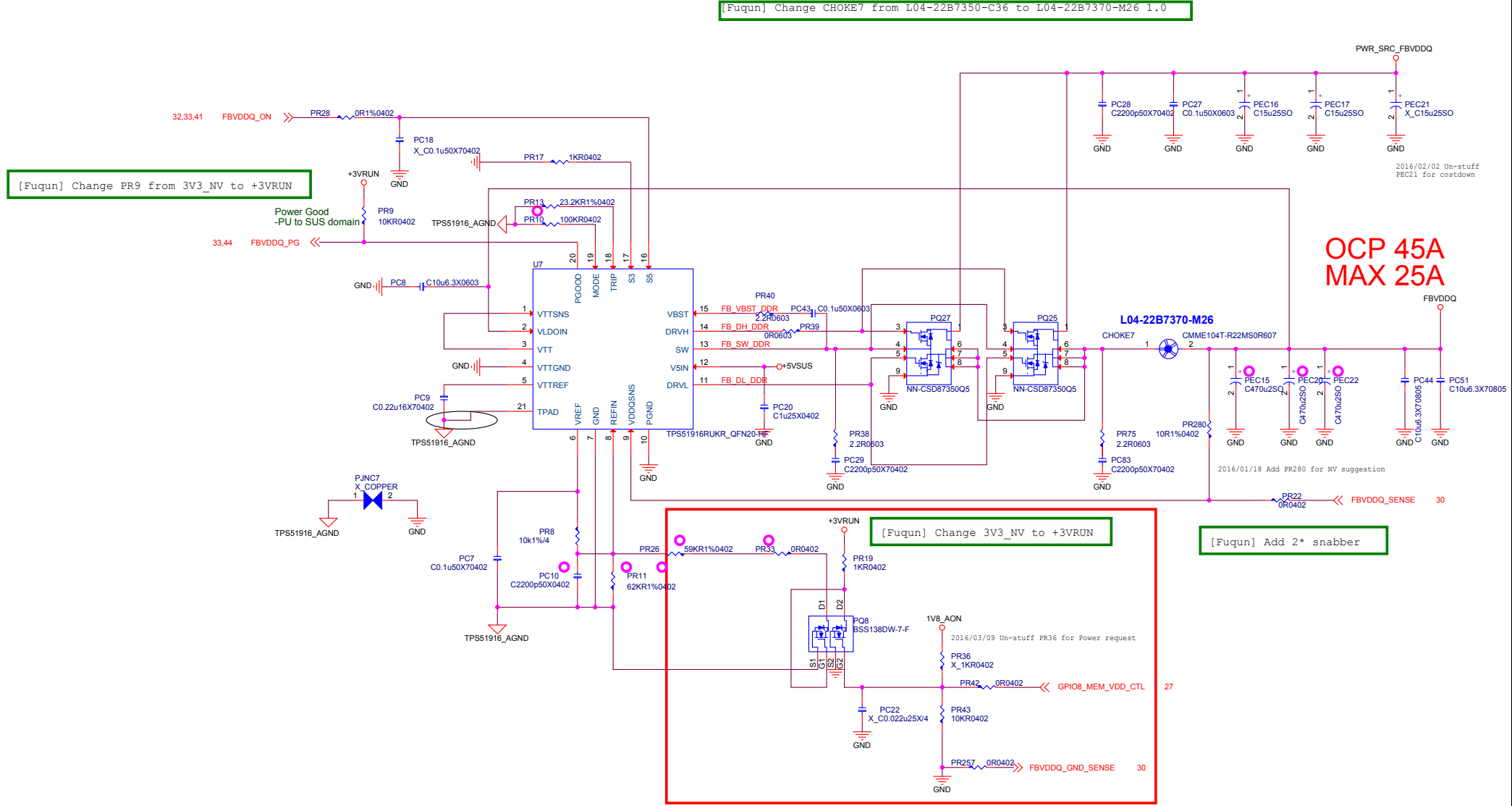
Voltage = 1.0V  
Current = 3A  
OCP(typi) = 4.8A

APL5930KAI-TRG\_SOP8-HF

I31-0593002-A30

[Fuqun] Change PEX\_VDD\_EN from NVDDS\_EN to NVDDS\_PG

msi MICRO-STAR INT'L CO.,LTD.	
Title	1VSUS /PEX_VDD/1.2VSUS
Size	Document Number
Date	Monday, June 20, 2016
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Rev	0A





# DGPU POWER / UP9509P

EDP-Peak 145A

EDP-Con 58A

# DGPU POWER NVVDD

VBoot:0.8V

Vmin:0.5V / Vmax:1.25V

[Fuqun] Change CHOKEl1/12/14 from L04-22B7350-C36 to L04-22B7370-M26 1.0

[Fuqun] Change PR115 from 3V3\_NV to +3VRUN

2016/01/18 NV suggest stuff PR249, un-stuff PR248  
2016/03/09 Modify PR249 to 10K ohm for Power request  
2016/04/07 Modify PR117, PR118 to R11-0621T12-Y01 for Power request  
2016/05/12 Modify PR118 to R11-0102T12-Y01 for Power request

[Fuqun] PR111 0ohm to 2.2ohm

2016/02/02 Un-stuff  
PEC23 for costdown

2016/04/07 Modify  
PR123 to  
R11-0304T12-Y01 for  
Power request

2016/04/07 Modify  
PR119, PR113 to  
R11-0000013-W08  
for Power request

2016/04/08 Modify  
PR112 to  
R11-0203T12-Y01 for  
Power request

2016/04/08 Modify  
PR130 to  
R11-0153T12-Y01 for  
Power request

2016/01/18 NV suggest stuff PR276, PR277

CONFIG	PR283	PR281	PR280	PR279	PR282	PC261
N17E-G1	R1	R2	R3	R4	R5	C
	6.19K	20.5K	4.32K	16.5K	309R	1.5nF

2016/04/08 Modify  
PR130 to  
R11-0153T12-Y01 for  
Power request

2016/02/02 Un-stuff  
PEC25 for costdown

[Fuqun] Add 3\* snabber

DGPU POWER / UP1666P

EDP-Peak 74A

EDP-Con 28A

[Fuqun] NC PR18/Mount PR20 1.0

DGPU POWER NVVDDS

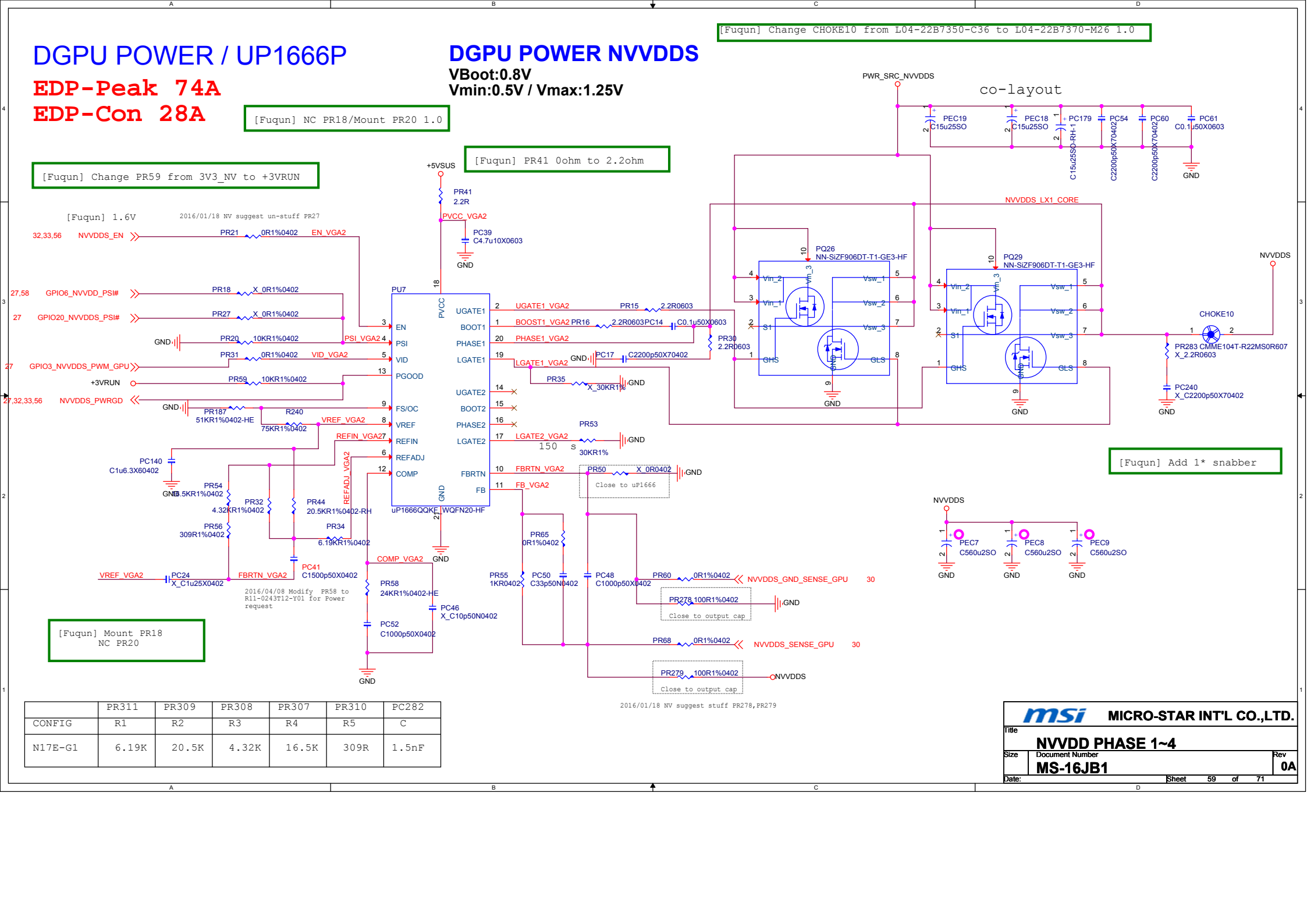
VBoot:0.8V

Vmin:0.5V / Vmax:1.25V

[Fuqun] PR41 0ohm to 2.2ohm

[Fuqun] Change PR59 from 3V3\_NV to +3VRUN

[Fuqun] Change CHOKE10 from L04-22B7350-C36 to L04-22B7370-M26 1.0



[Fuqun] 1.6V 2016/01/18 NV suggest un-stuff PR27

32,33,56 NVVDDS\_EN >> PR21 0R1%0402 EN VGA2

27,58 GPIO6\_NVVDD\_PSI# >> PR18 X 0R1%0402

27 GPIO20\_NVVDDS\_PSI# >> PR27 X 0R1%0402

GND PR20 10KR1%0402 PSI VGA2 4

27 GPIO3\_NVVDDS\_PWM\_GPU >> PR31 0R1%0402 VID VGA2

+3VRUN PR59 10KR1%0402

27,32,33,56 NVVDDS\_PWRGD << GND PR187 51KR1%0402-HE R240 75KR1%0402

VREF VGA2 PC140 C1u6.3X60402 GND PR54 5KR1%0402 PR32 4.32KR1%0402 PR56 309R1%0402

REFIN VGA2 PR44 20.5KR1%0402-RH PR34 6.19KR1%0402

REFADJ VGA2 PR41 C1500p50X0402

COMP VGA2 PR58 24KR1%0402-HE PC46 X\_C10p50N0402

PC52 C1000p50X0402

PC24 X\_C1u25X0402

FBRTN VGA2

2016/04/08 Modify PR58 to R11-0243T12-Y01 for Power request

[Fuqun] Mount PR18 NC PR20

2016/01/18 NV suggest stuff PR278, PR279

Close to uP1666

Close to output cap

Close to output cap

Close to output cap

Close to output cap

Close to output cap

Close to output cap

Close to output cap

Close to output cap

Close to output cap

Close to output cap

Close to output cap

Close to output cap

	PR311	PR309	PR308	PR307	PR310	PC282
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	1.5nF

co-layout

NVVDDS\_LX1\_CORE

[Fuqun] Add 1\* snabber

MICRO-STAR INT'L CO.,LTD.

Title

NVVDD PHASE 1~4

Size

Document Number

MS-16JB1

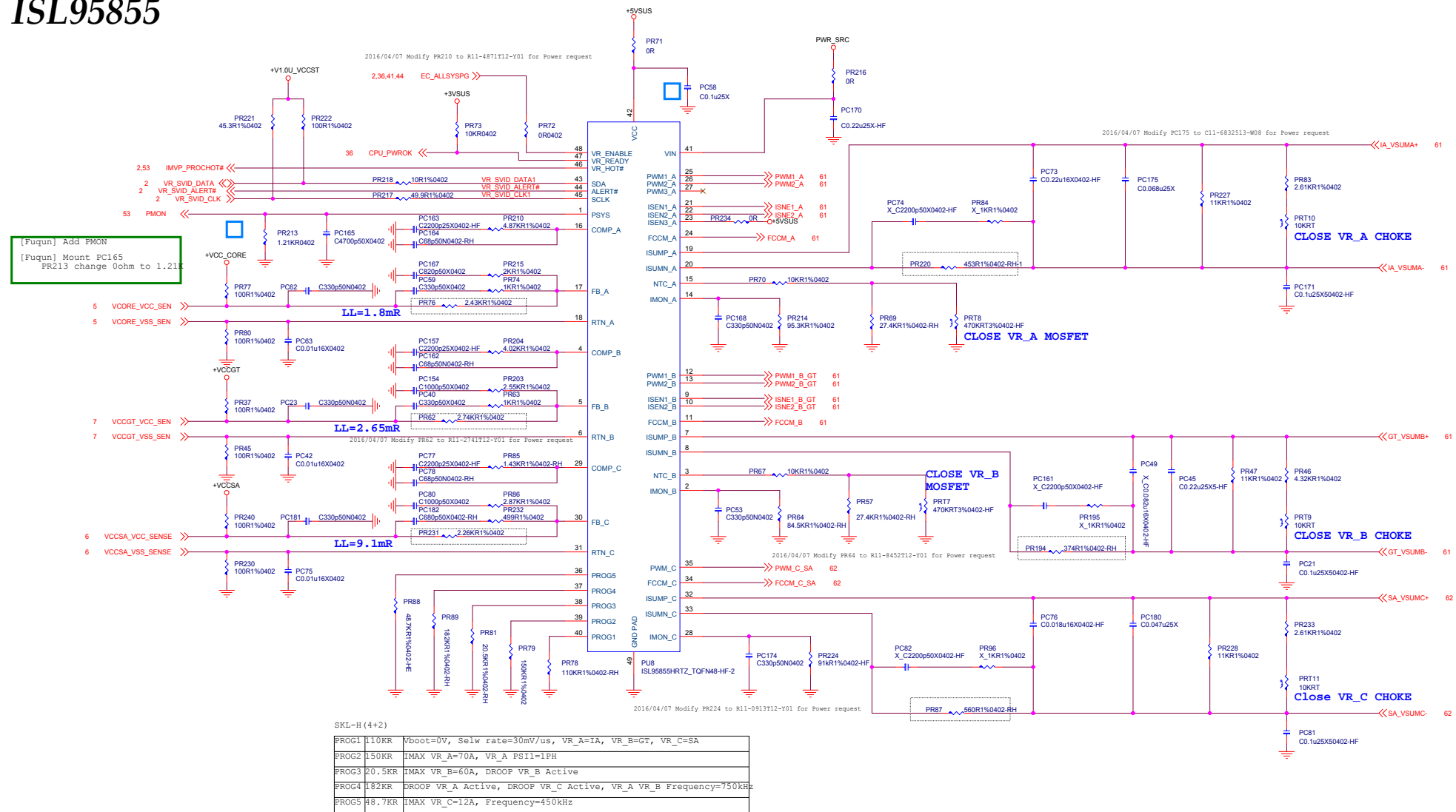
Date:

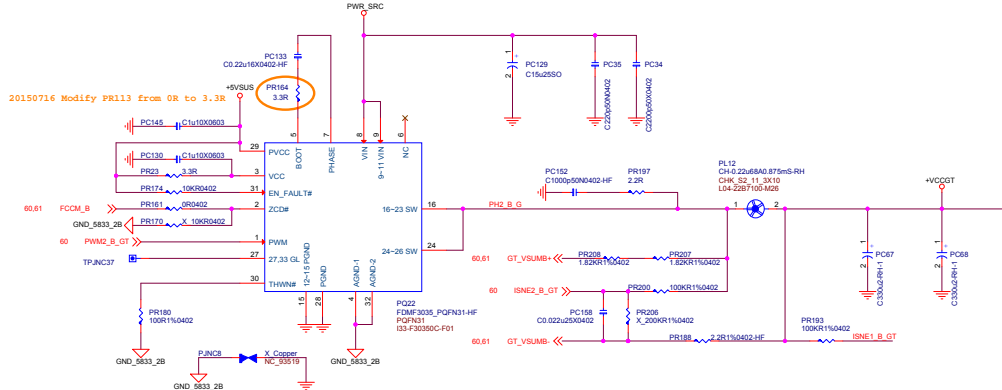
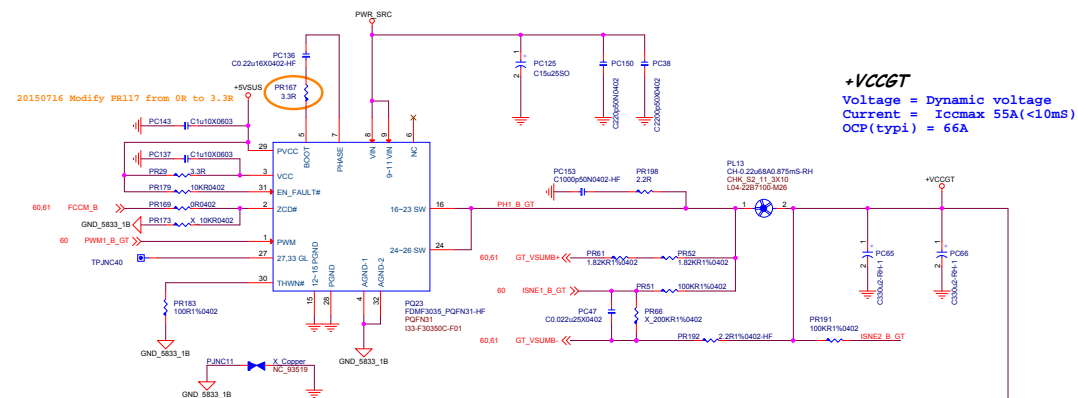
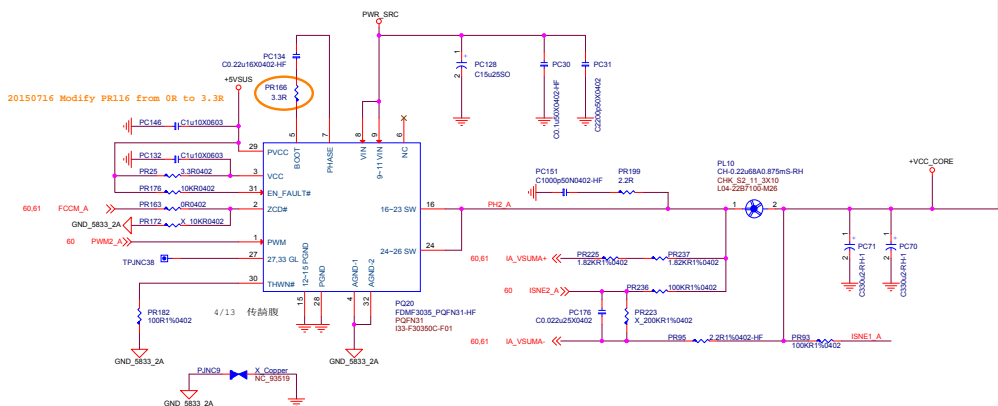
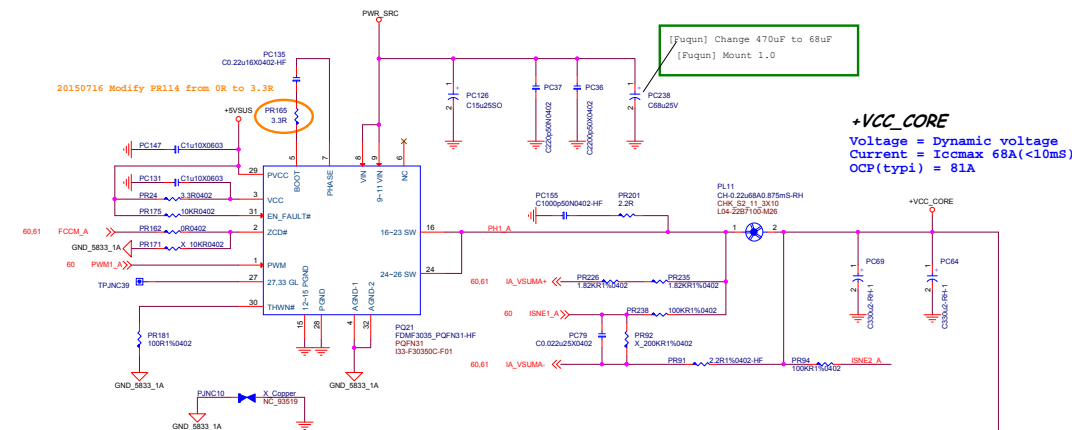
Sheet 59 of 71

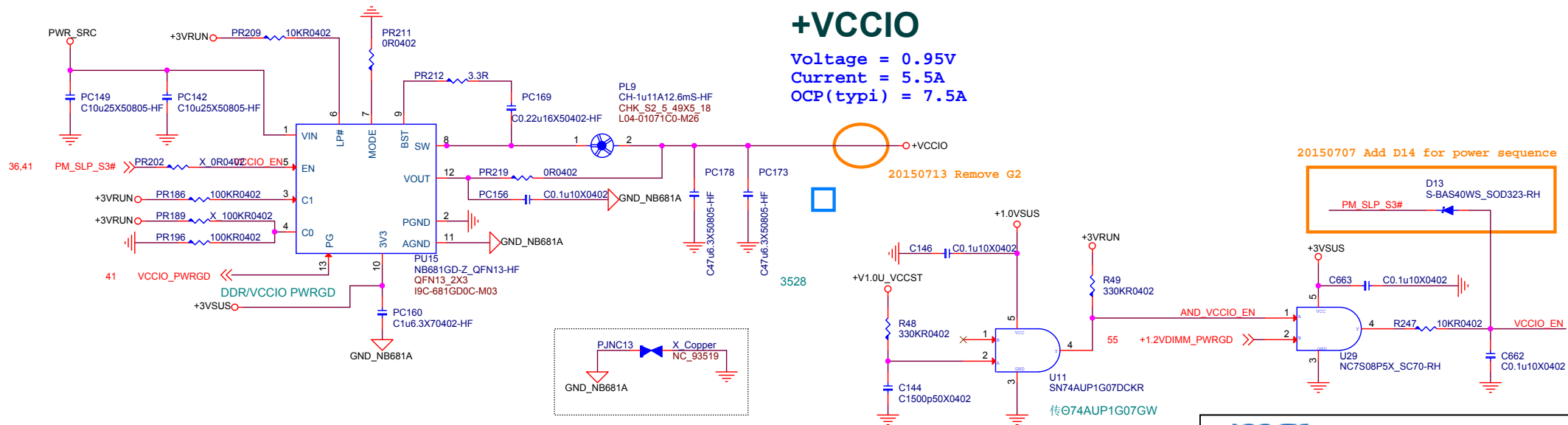
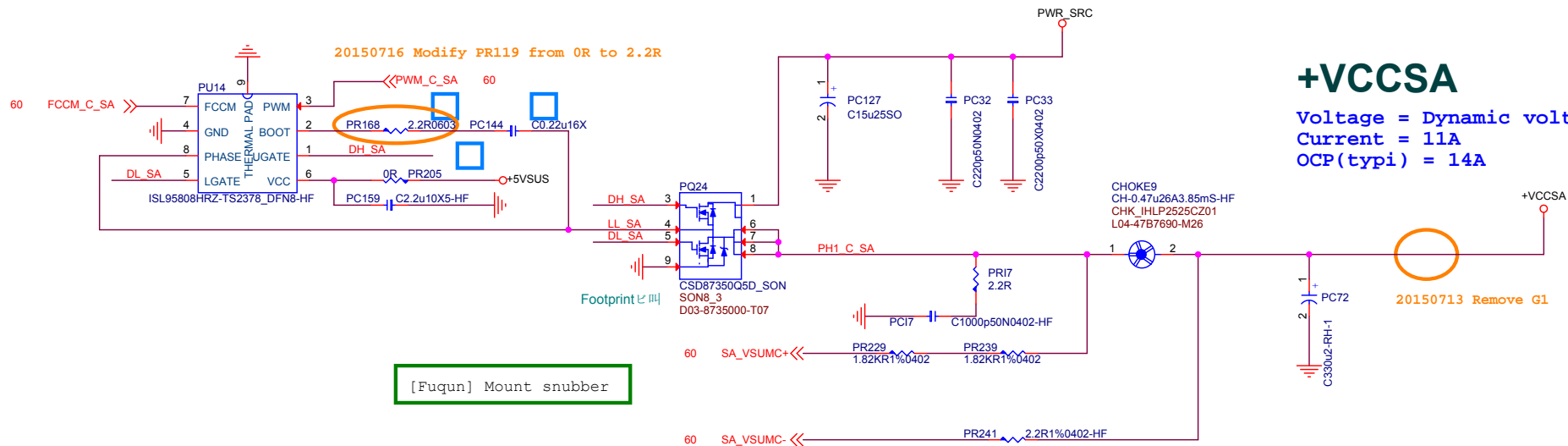
Rev 0A

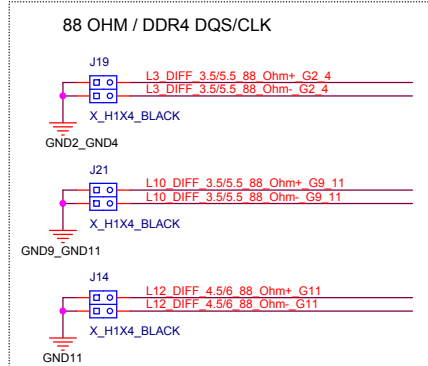
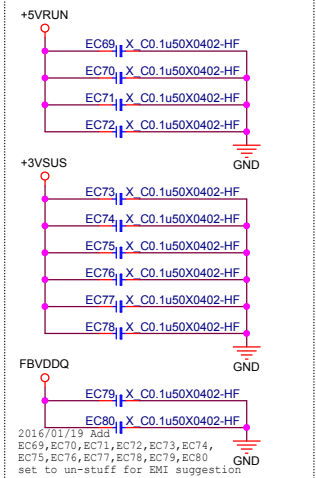
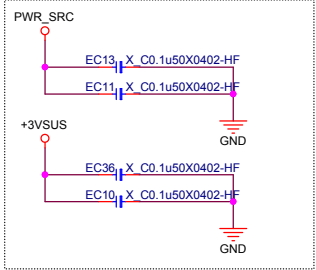
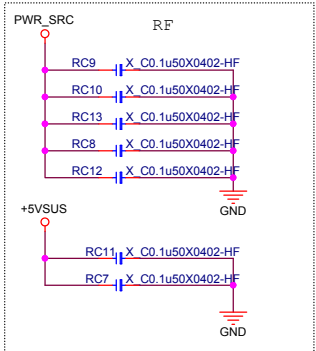
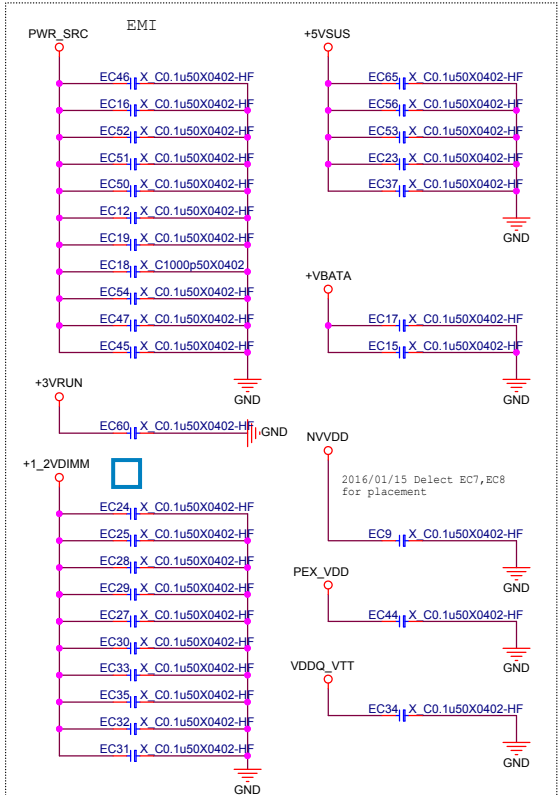
# Skylake H-line 42 45W

## ISL95855

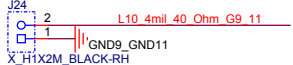
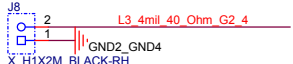




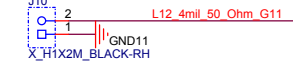
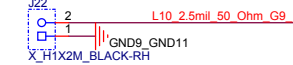
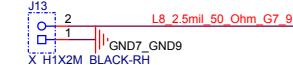
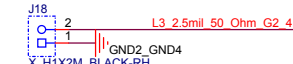
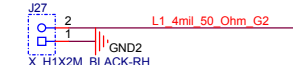




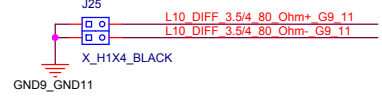
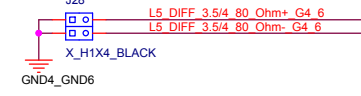
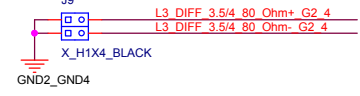
**40 OHM DDR4 CMD/CTRL/CKE/ALERT**



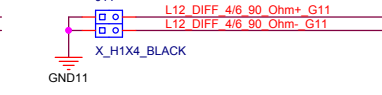
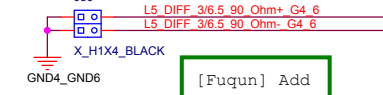
**50 OHM / DDR4 DQ**



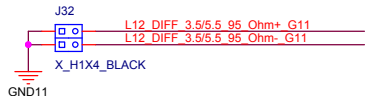
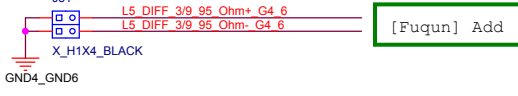
**80 OHM GDDR5 CK/WCK**



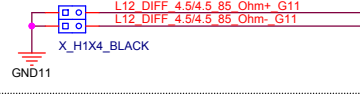
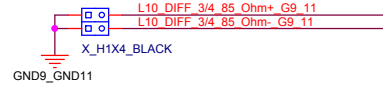
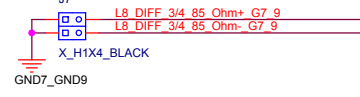
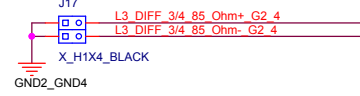
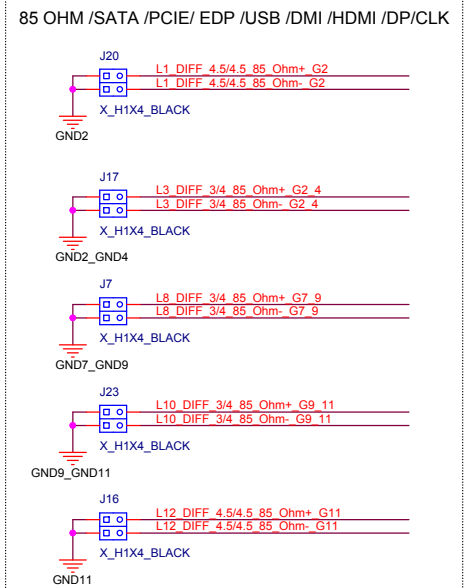
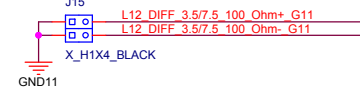
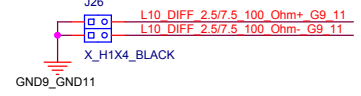
**90 OHM / XTAL(GPU)**

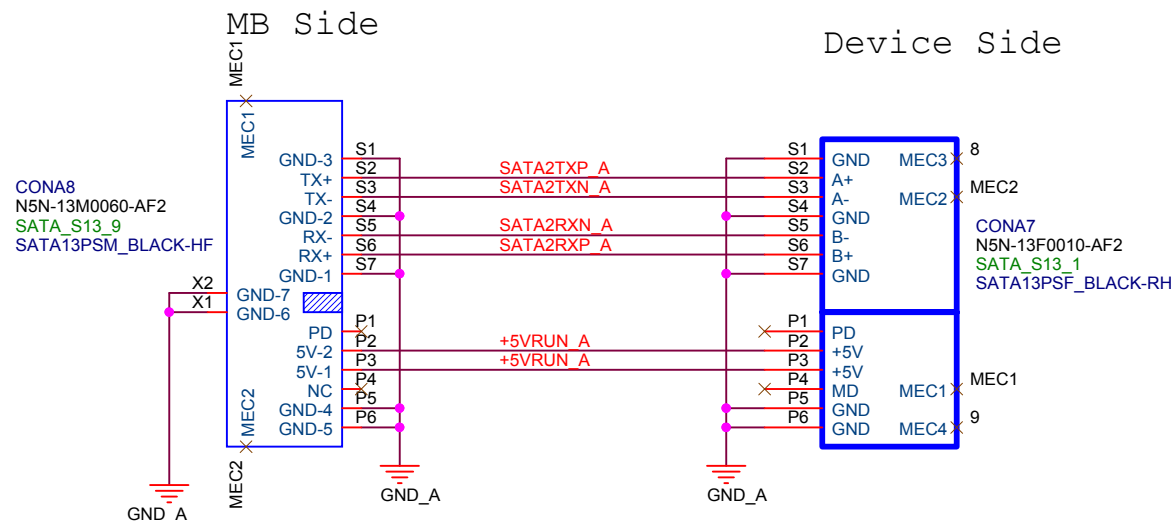


**95 OHM / HDMI**

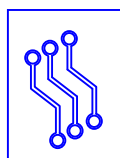


**100 OHM / LAN /HDMI (After DP139)**





# PCBA1

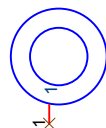


PD0-16J8B0A-H73

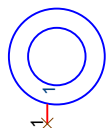
**PD0-16JBA10-H73**

Hannstar: PD0-16J8A0B-H73  
TRIPOD: PD0-16J8A0B-T53

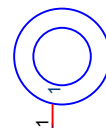
HB10  
X\_NPTH\_80  
NPTH\_80



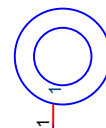
HB7  
X\_NPTH\_80  
NPTH\_80



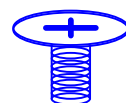
MB7  
X\_H\_R197D91  
H\_R197D91



MB8  
X\_H\_R197D91  
H\_R197D91



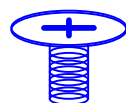
SCREWA2



**E43-1205003-H29**

SKEW

SCREWA1



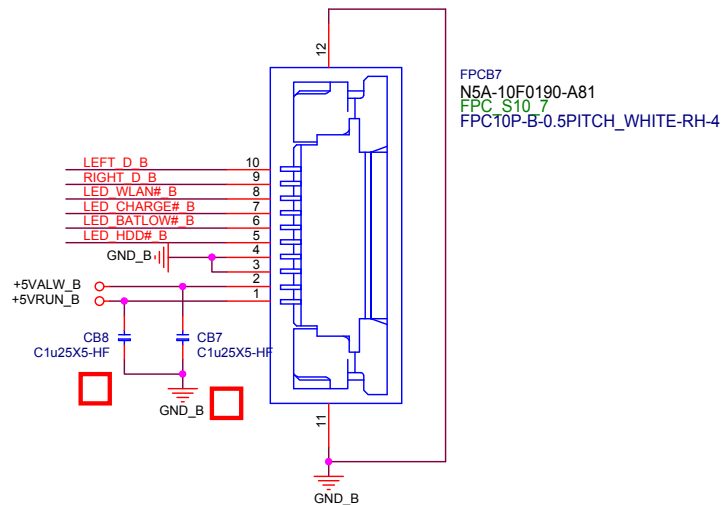
**E43-1205003-H29**

SKEW

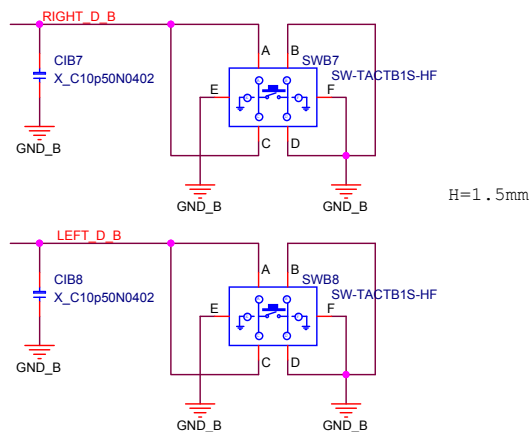
**msi**

**MICRO-STAR INT'L CO.,LTD.**

Title		
<b>[A] 1798 ODD</b>		
Size	Document Number	Rev
A4	<b>MS-16JBA</b>	0A
Date:	Monday, June 20, 2016	Sheet 65 of 71



1798



1798

LED FRONT

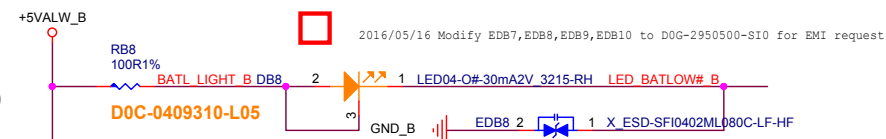
BLUE (HDD)



BLUE (WLAN)



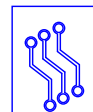
ORANGE (BATLOW)



BLUE (CHARGE)



PCBB1



PD0-16JBB0A-H73  
PD0-16JBB10-H73

Hannstar: PD0-16J8B0B-H73  
TRIPOD: PD0-16J8B0B-T53



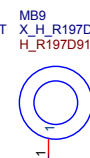
HB9  
X\_NPTH\_80  
NPTH\_80



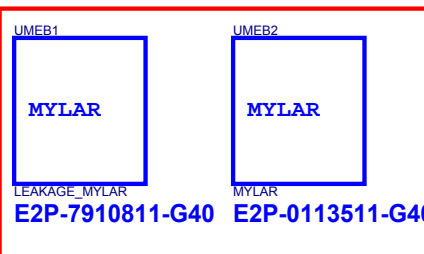
HB8  
X\_NPTH\_80  
NPTH\_80



MB10  
X\_H\_R276D118\_PT  
H\_R276D118\_PT



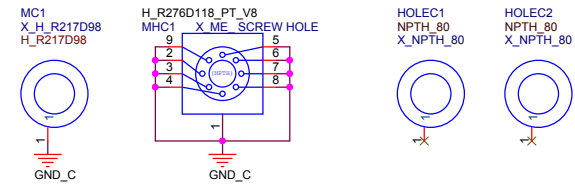
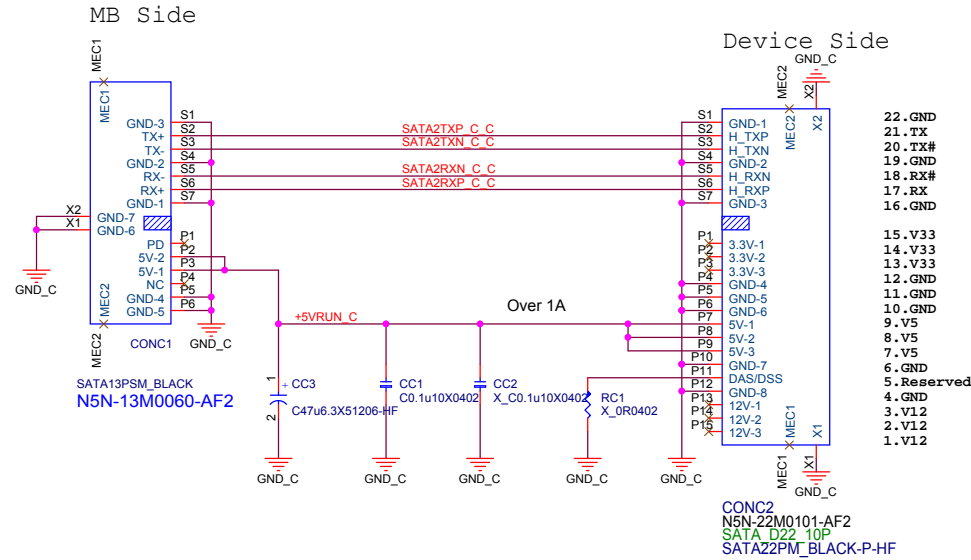
MB9  
X\_H\_R197D91  
H\_R197D91



msi MICRO-STAR INT'L CO.,LTD.			
Title [B] 1798 LED/ TP			
Size B	Document Number	Rev 0A	
Date:	Monday, June 20, 2016	Sheet	66 of 71



Verge SATA HDD

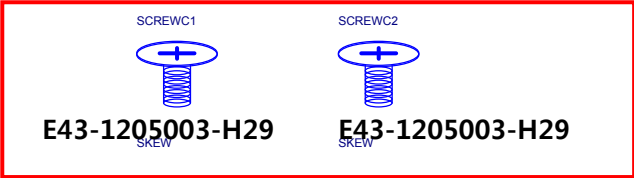


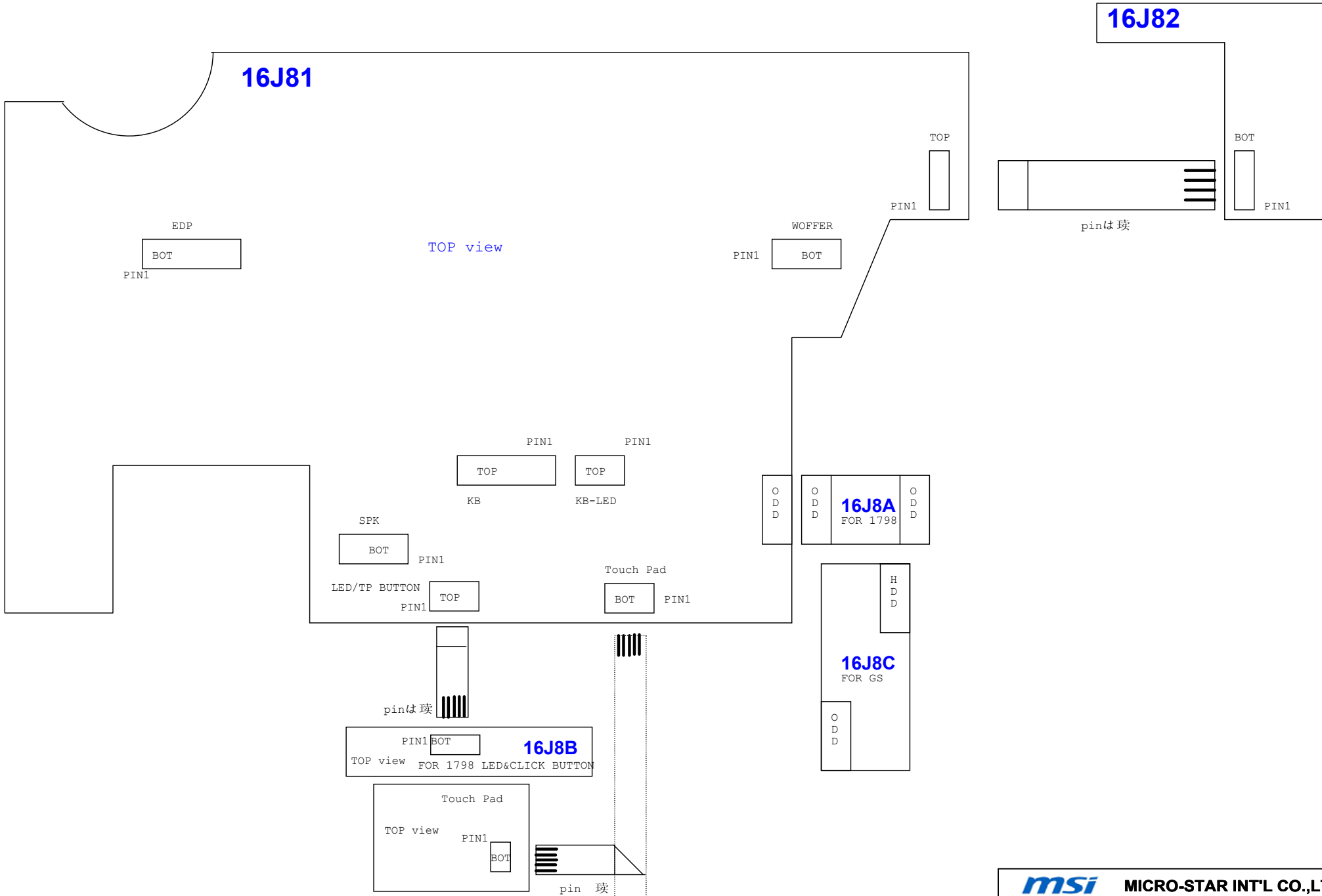
PCBC1



PD0-16JBC0A-H73  
PD0-16JBC10-H73

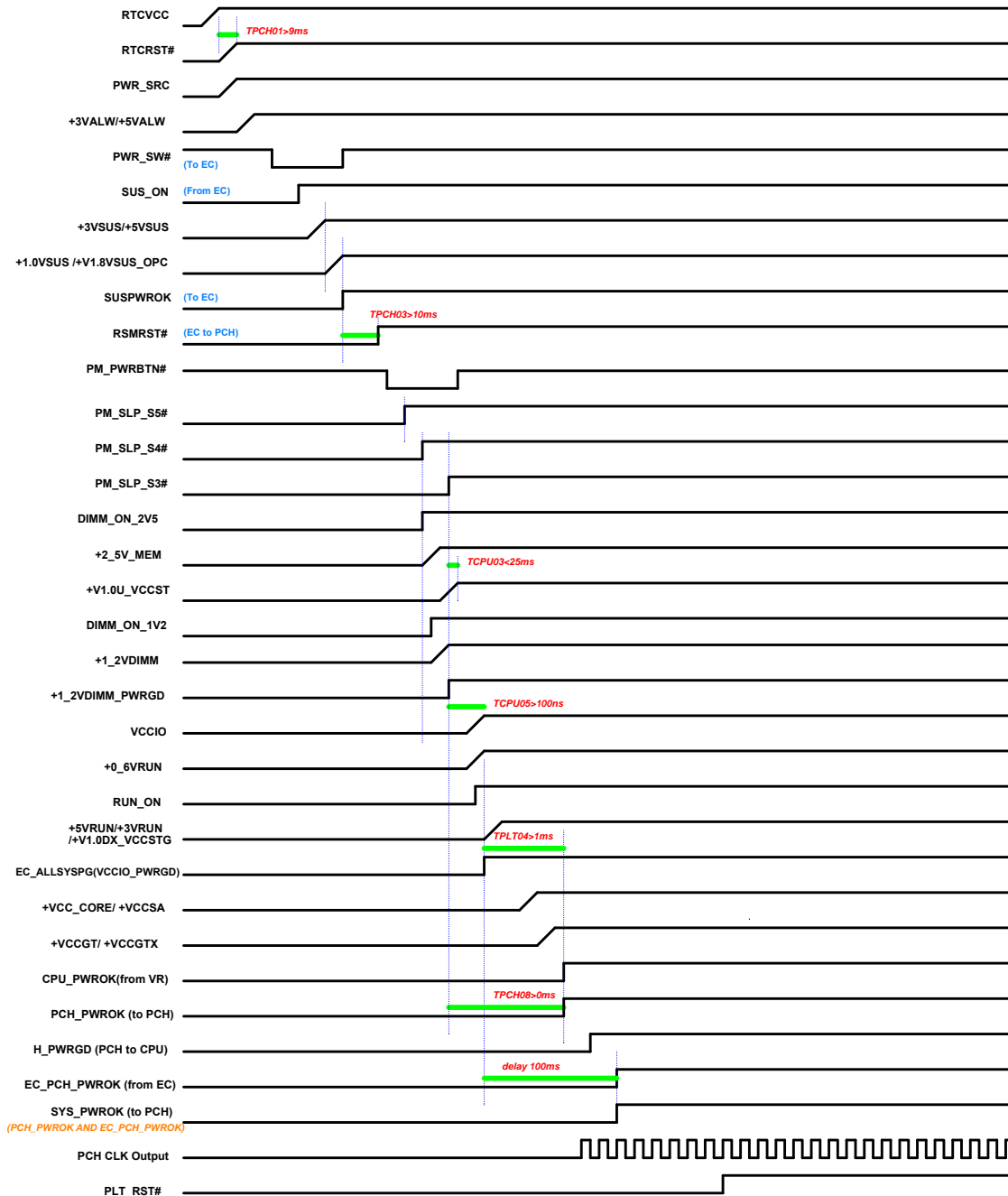
Hannstar: PD0-16J8C0B-H73  
TRIPOD: PD0-16J8C0B-T53





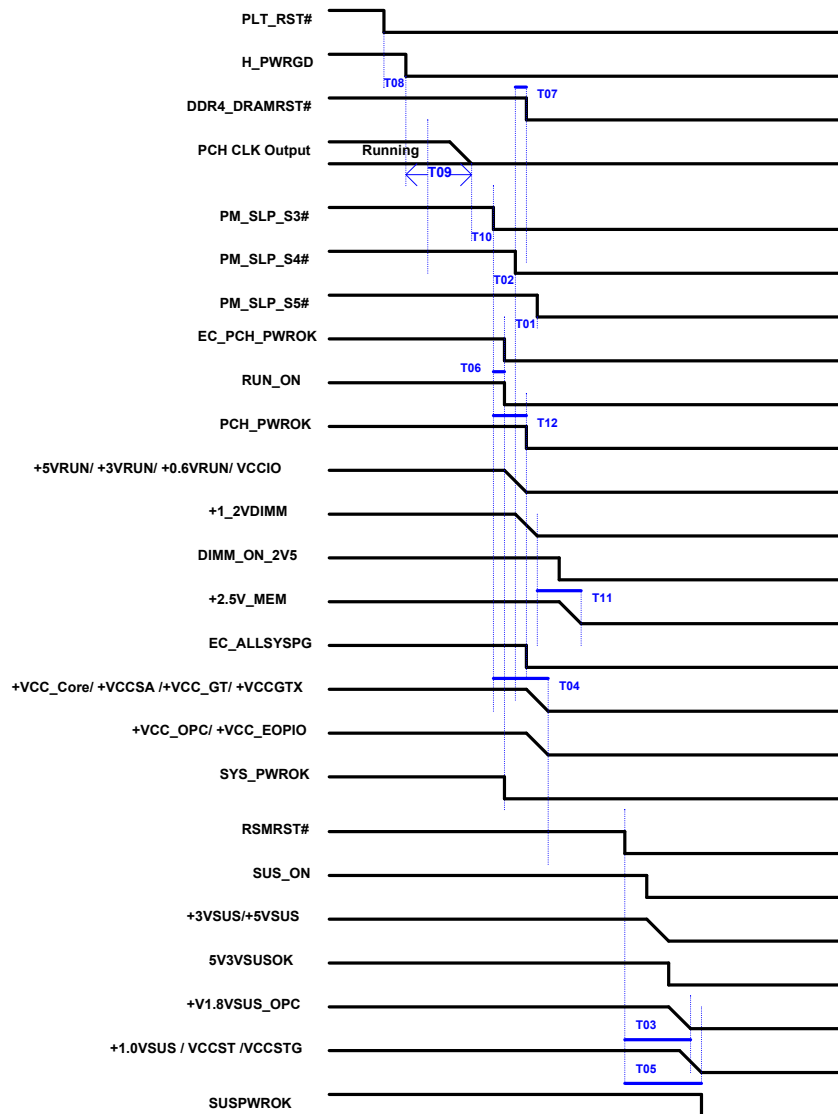
# Power on Sequence

G3 -> S0



# Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

History

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Page	Description	Page	Description	Page	Description	Page	Description
2	Change R266/R268 from 0ohm to 75ohm follow intel DG	33	Add reserved U62/C2811				
4	Remove CPU HDMI/DP bus		Change R336 from 4.02K to 2K				
	Remove PCH to CPU AUDIO bus		Change R500/R570 from 20K to 10K				
6	Remove reserved 1.0VSUS to +V1.0DX_VCCSTG/+V1.0U_VCCST LDO	32	Add reserved R478				
10	NC R90/Q9, Add Q47	44	Add R3/R5/R370/R595/Q5/Q64/C2				
	Cahnge C2821 from 1u to 0.1u follow NV DG		Change R68/R98 PU from NV3V3 to +3VRUN				
18	Change LB8 ESR from 0.03ohm to 0.01ohm follow NV DG	45	Add R586/R588/R368/R364/2839/Q50				
24	Add NV display port A/B		Change R351/R343 PU from NV3V3 to +3VRUN				
25	Add NV display port C/D						
26	Add NV display port E/F						
27	Add GPIO 14/15/17/18/24/27						
	NC R309, Add R300/R317/R490						
28	Add R492 and CORE_PLLVDD power						
29	Change NV STRAP3 from LOW to High for enable NV VGA						
32	Connect GPIO28_OC_WARN_N to U8.8 pin						
	Add/change NVVDDS/PEX_VDD/1V8_MAIN dischaarge						
33	Re-draw NV power sequence follow kunshan N17 MXM design						
34	Remove HDMI/DP HPD/I2C bus in PCH						
35	Cahnge ASMI142 PCIE cap from 0.1u to 0.22u follow vender DG						
	L_LDRQ0# add PU 10Kohm						
	Remove 33M CLK buffer, remove LPC debug card						
	Add HDMI/DP HPD from connector						
36	Remove PCH to CPU audio bud						
	Add R409/R503 for system power sequence						
37	Change BIOS footprint to correct						
38	Add 2pcs 1.0VSUS CAP, 2pcs 3VSUS CAP						
39	Add C958						
41	Remove LPC debug card						
	Change battery charge control function						
	Add HDMI/DP detect function						
	Add 506						
42	Cahnge ASMI142 PCIE cap from 0.1u to 0.22u follow vender DG						
	Add D24 follow verser DG						
43	Add USB POWER PROTECT CIRCUIT						
44	Add DP re-driver IC						
45	Change HDMI re-driver from 1.4b to 2.0						
46	Change 3pcs AGND to GND cooper to cap						
48	Change R78 from 10K to 30K follow vender DG						
	Add 1pcs 3VLAN CAP						
49	NC U31/U35						
51	Add R513						
	Mount TPM in 0A PCBA						
52	Add USB POWER PROTECT CIRCUIT						
53	Change battery charge IC						
54	Add 1.1VRUN for HDMI2.0 re-driver IC						
56	Change PEX_VDD_EN from NVDDS_EN to NVDDS_PG						
	Change PEX_VDD_PG PU from NV3V3 to +3VRUN						
	Add 1V8_AON_PG (PU7 pin-7)						
57	Change PR9/PR19 PU from 3V3_NV to +3VRUN						
	Add 2* snabber						
58	Change PR115 PU from 3V3_NV to +3VRUN						
	Add 3* snabber						
59	Change PR59 PU from 3V3_NV to +3VRUN						
	Add 1* snabber						
	Change PR41 from 0ohm to 2.2ohm						
	Mount PR18, NC PR20						
60	Connect PMON from charge IC						
	Mount FC165, PR213 change 0ohm to 1.21K						
61	Change PC238 from 470uF to 68uF						
62	Mount snubber						
63	Add 95ohm impadence						
67	Change ODD connect ORCad LIB						